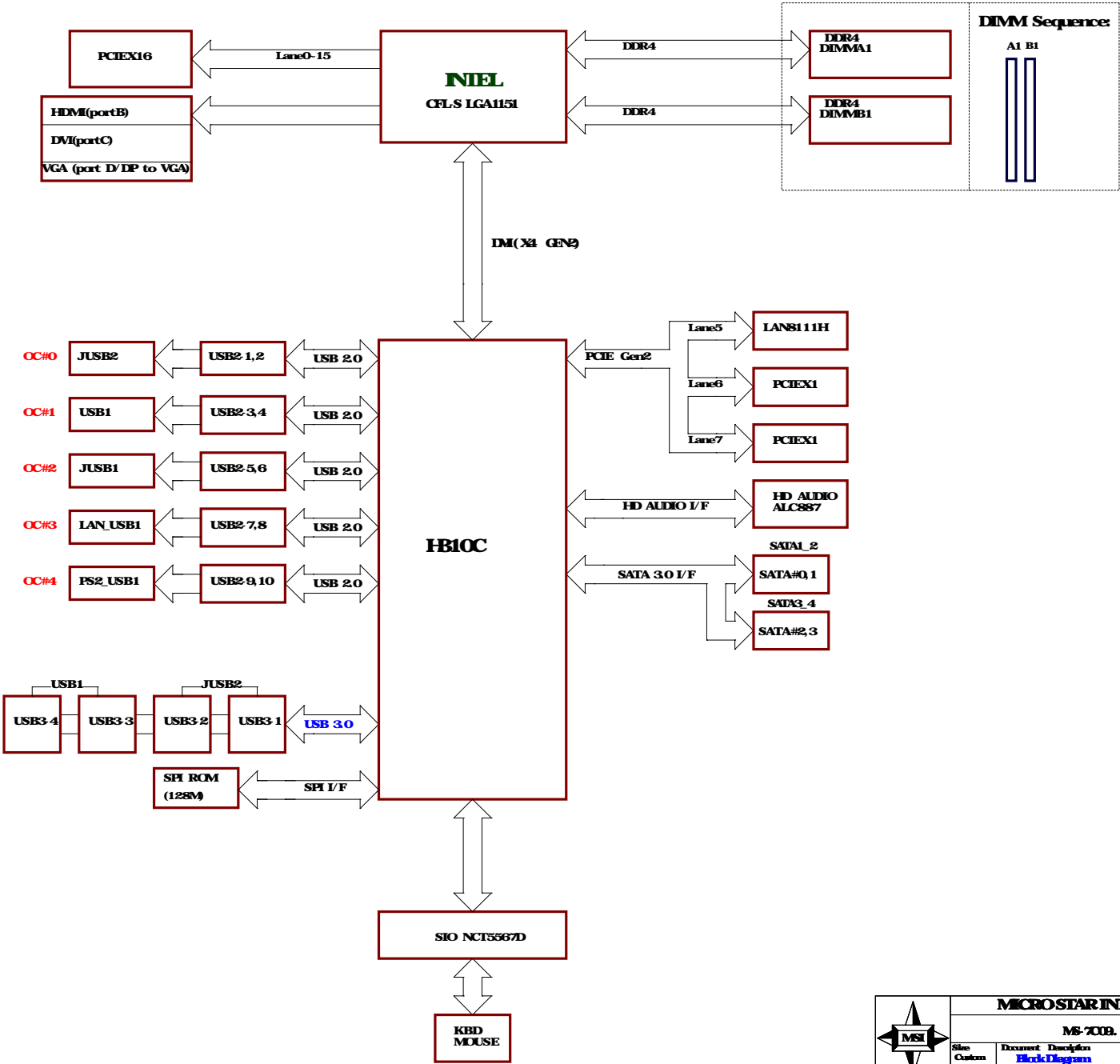
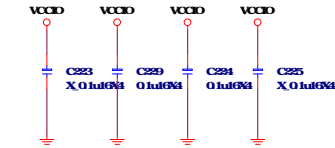
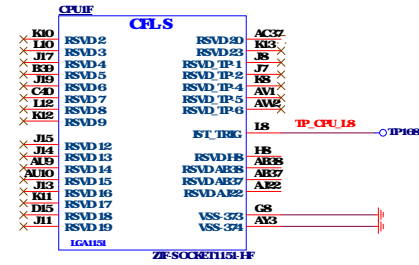
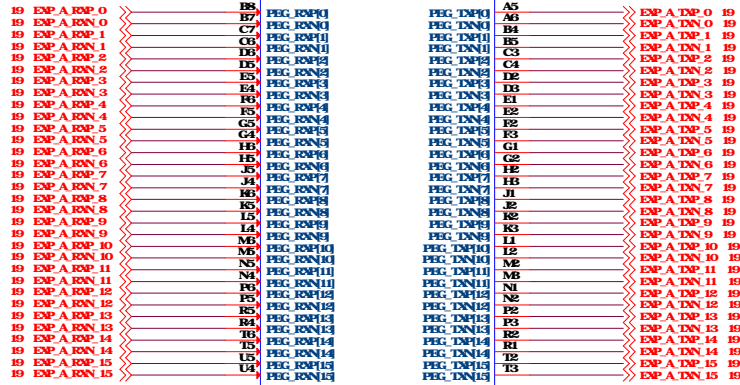
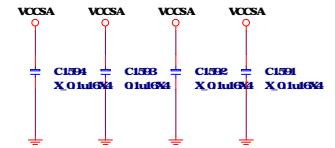


MS-7009 Block Diagram

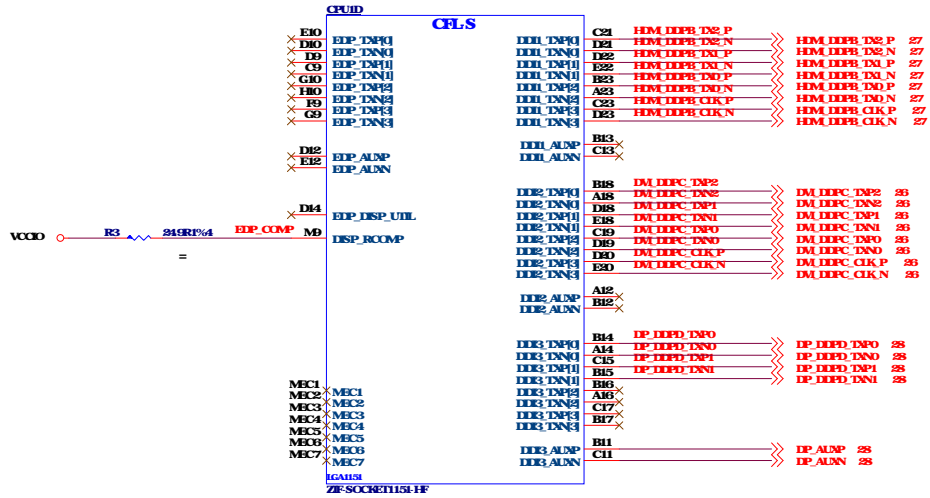




For RIE reference VCCIO USE
please close to RIE via side



For DM reference VCCSA USE
please close to DM via side



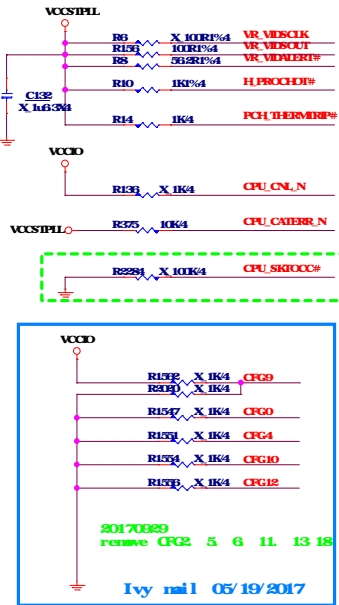
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MICROSTAR INT'L CO., LTD

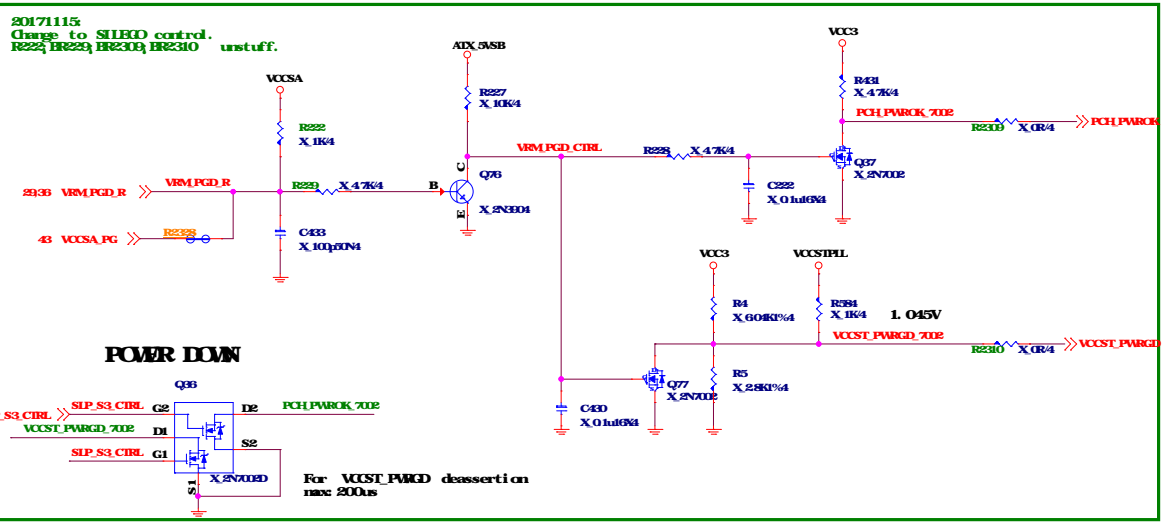
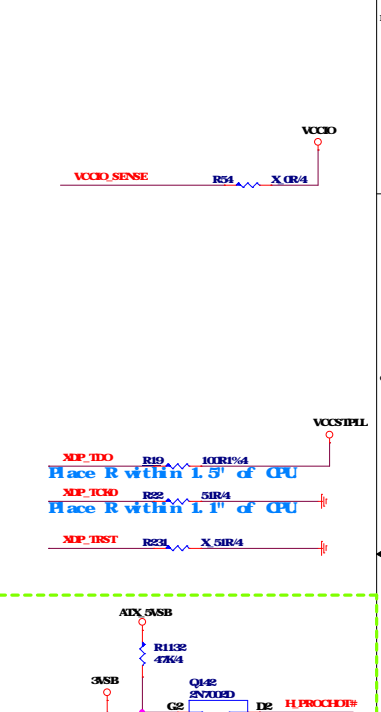
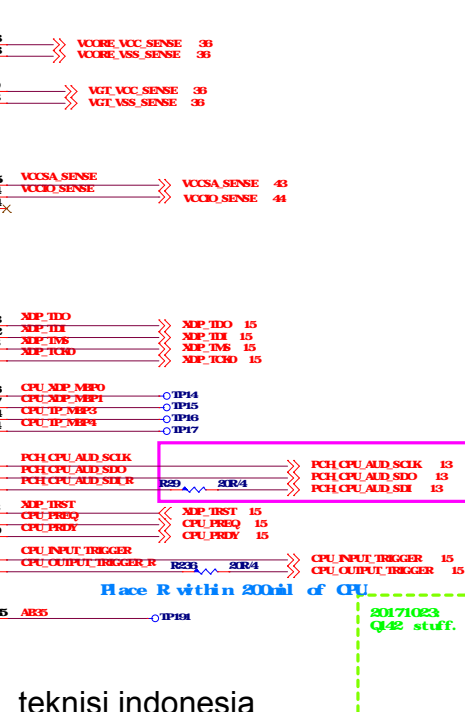
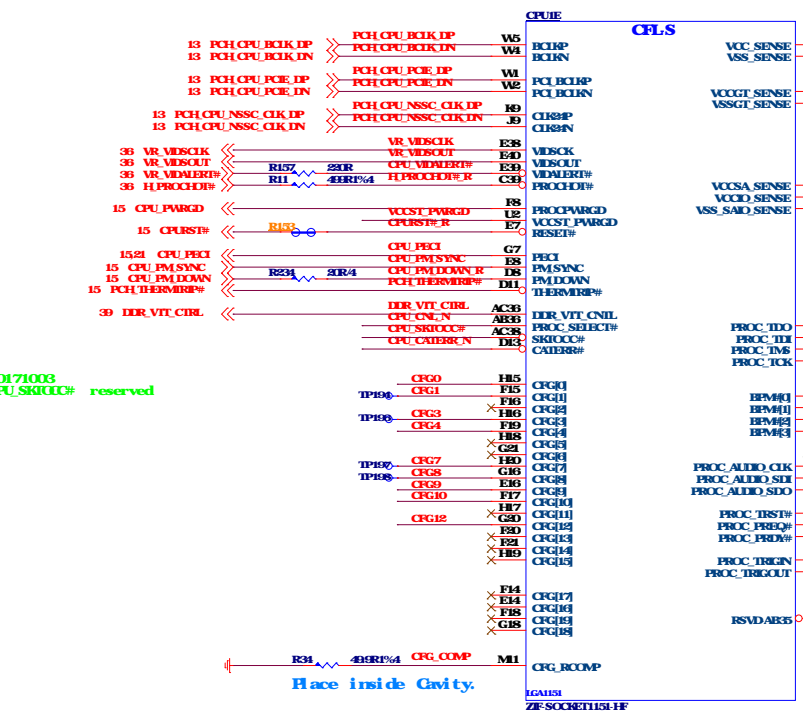
MS-700B

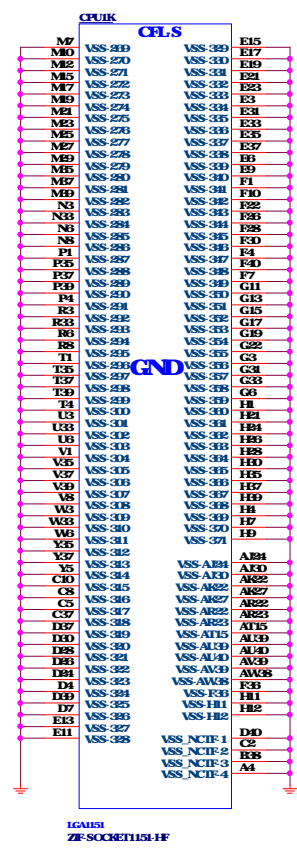
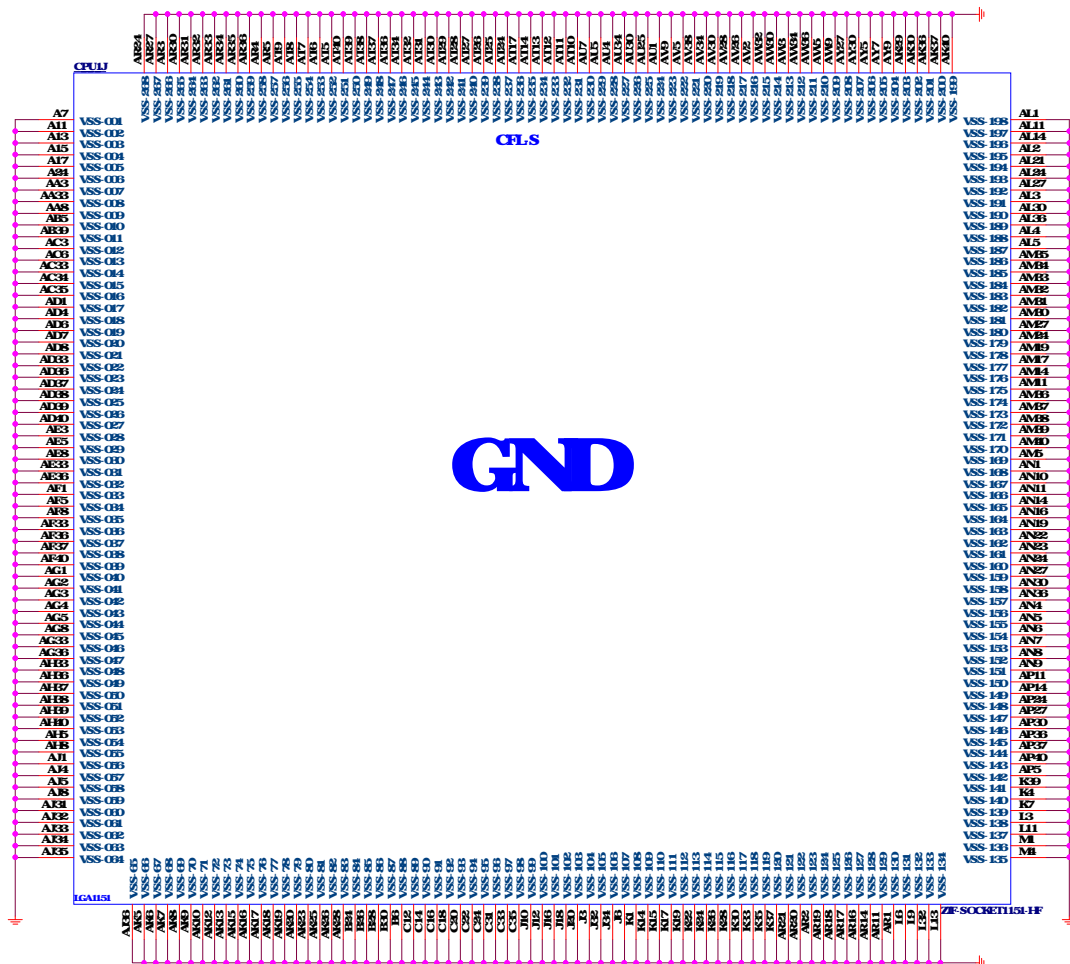
Site: Custom Document: Description: CPU-PEG/Display

Date: Tuesday, March 24, 2009 Sheet: 4 of 02

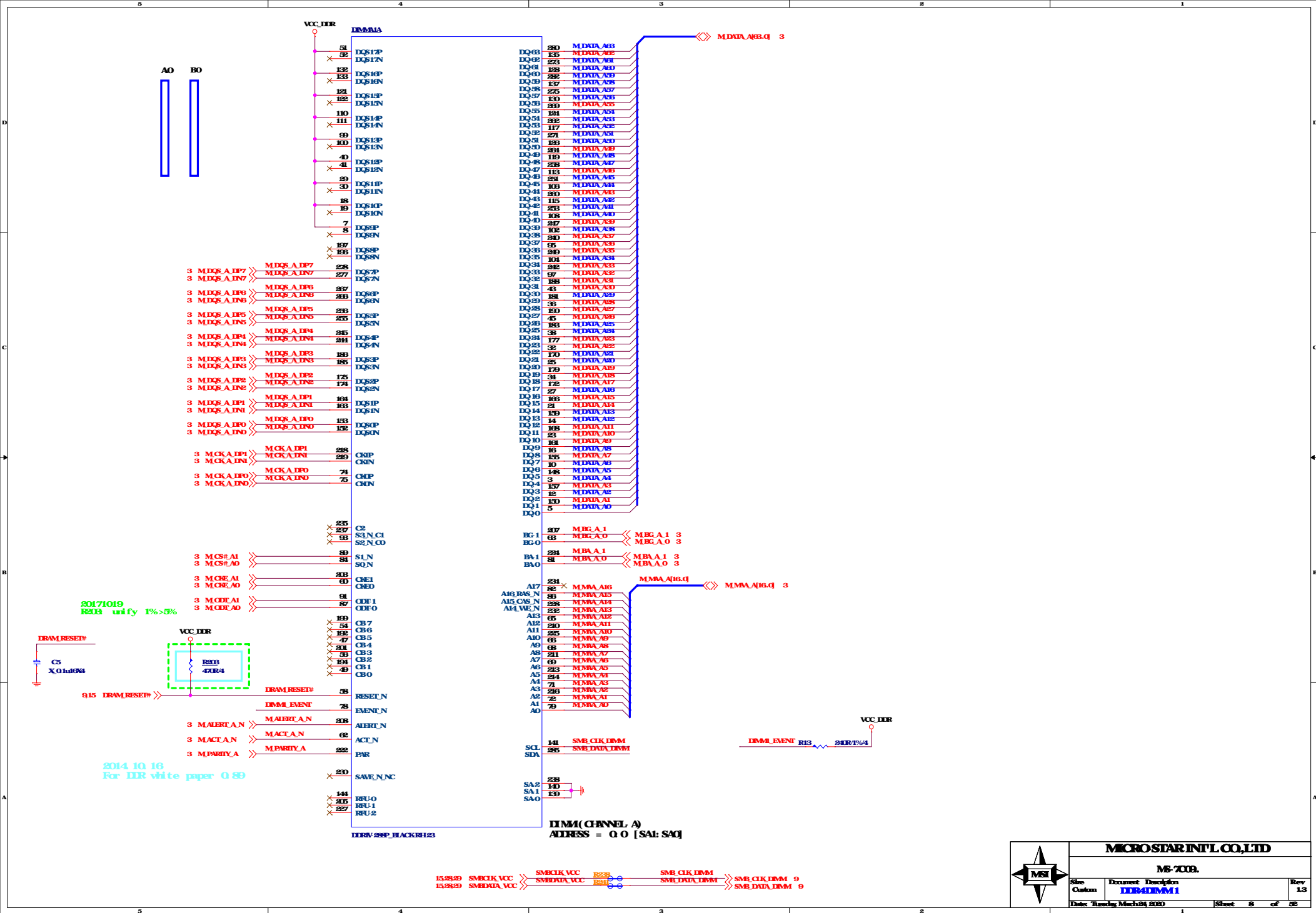


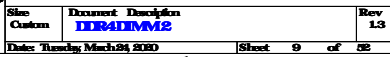
CFG Table		
HIGH	LOW	DESCRIPTION
0	No Lock	Lock
1		RSVD
2	NORM	REVERSE
3		RSVD
4	DISABLE	ENABLE
5	DISABLE	ENABLE
6	DISABLE	ENABLE
7	RESET	RSVD
8		RSVD
9		RSVD
10		RSVD
11		RSVD
12		RSVD
13		RSVD
14	RSVD	
15	RSVD	

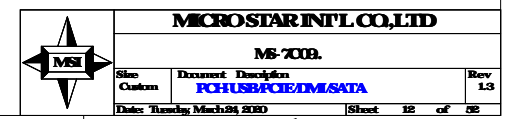




Vinafix.com



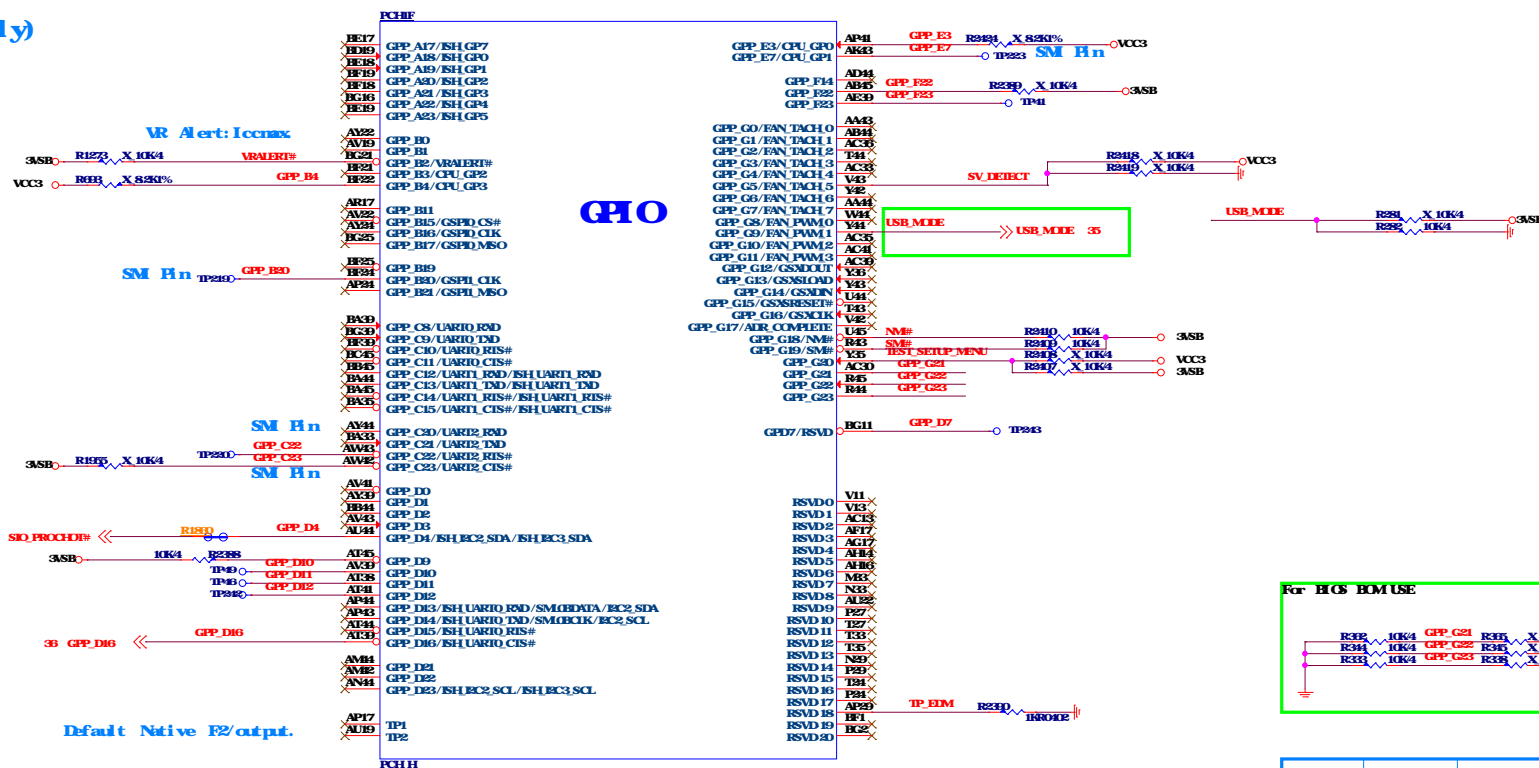





```

GPIQ SM/NM):
GPP_B14, GPP_B20, GPP_B23
GPP_C 23 22]
GPP_D 4 0
GPP_E 8 0
GPP_I 3 0
GPP_Q 7 0 (Support SM# only)

```



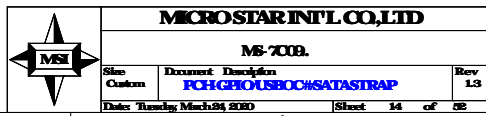
20171203
GPP_D16 pull low R1988 unstuff.

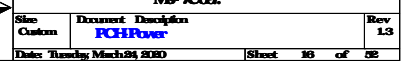
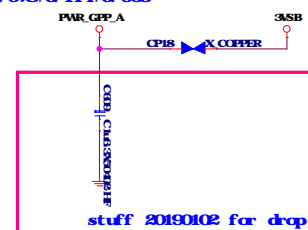
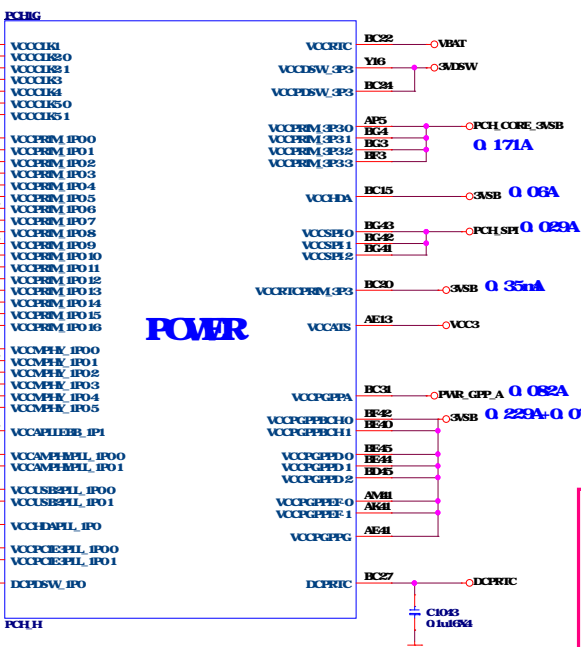
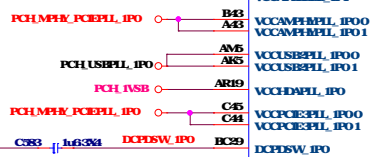
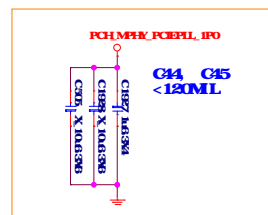
Default Native F2/output.

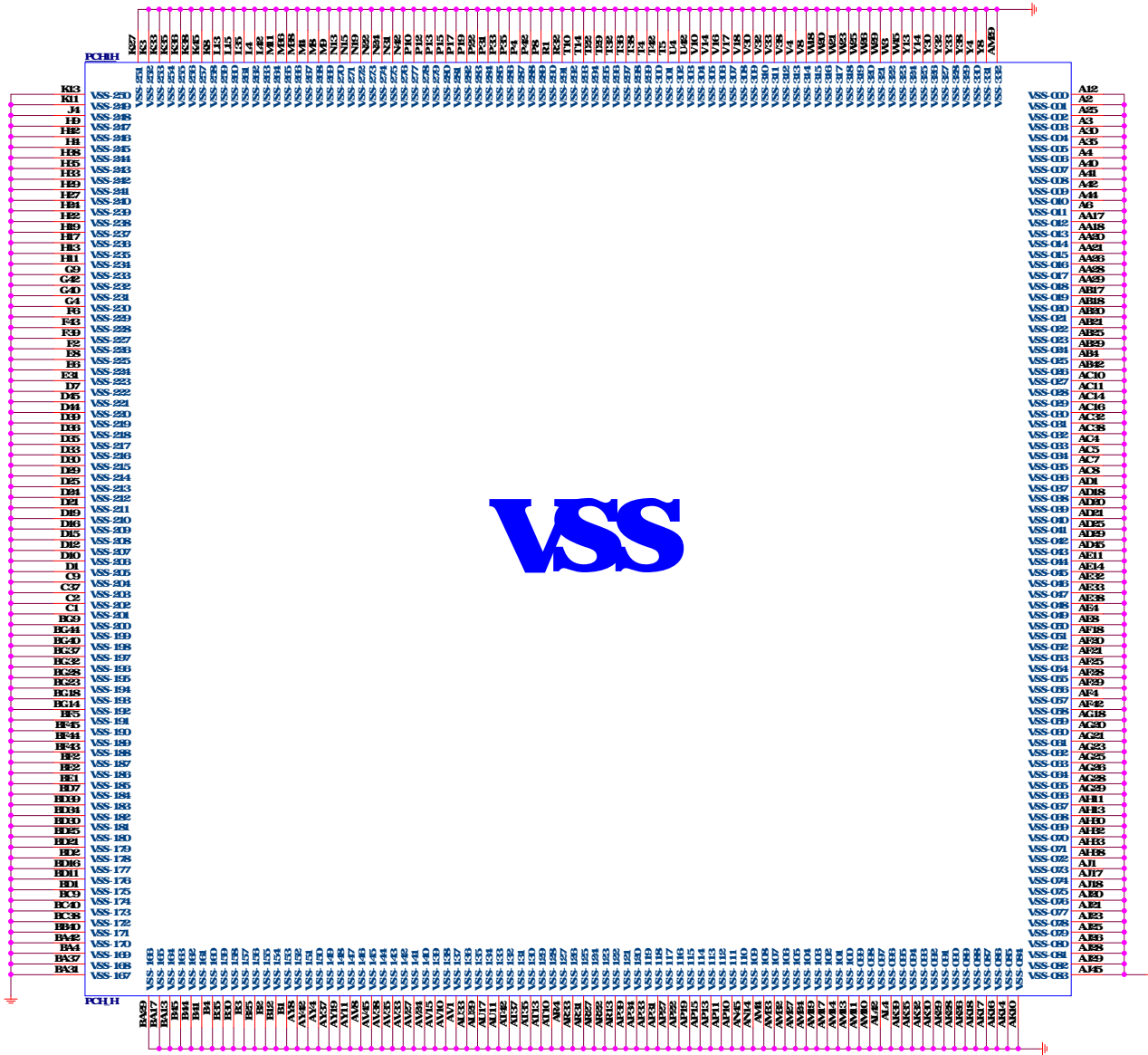
For HCS BOMUSE

The diagram shows a 3.3V supply connected to three resistors (R338, R344, R333) in parallel. Each resistor is labeled with a value of 10K/4. The circuit also includes three diodes (GPP_G21, GPP_G22, GPP_G23) and three resistors (R335, R345, R336) in parallel, each labeled with a value of X 10K/4. The output is labeled 3.3V.

	GPP_I 12	GPP_I 13	GPP_I 14
FB1Q_VH 0	0	0	0
FB1Q_VD 0	0	0	1





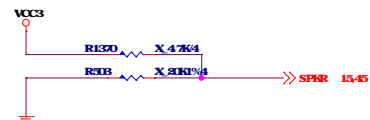


Vinafix.com



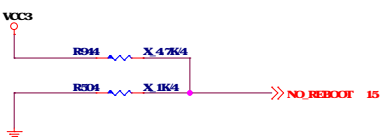
MICROSTAR INT'L CO., LTD		
MS-700B		
Site Custom	Document Description PCB LAYOUT	Rev 1.0
Date: Tuesday, March 24, 2020		Sheet 17 of 22

TOP Swap



Internal pull-down 20K is disabled after FLRST#

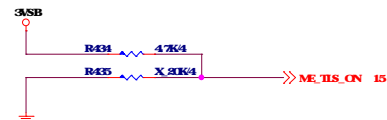
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after FLRST#

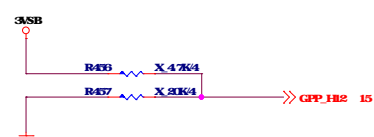
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMST

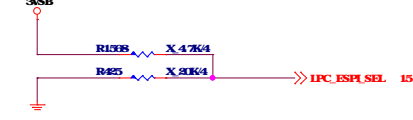
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMST

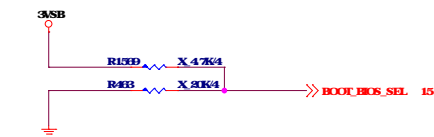
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMST

Boot BIOS



0 : SPI
1 : LPC

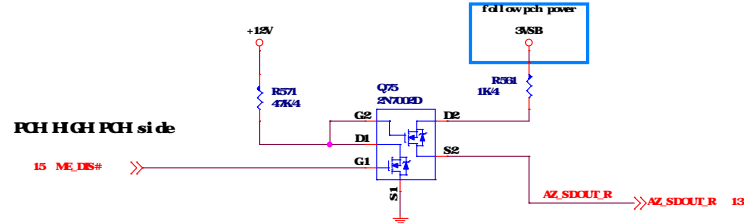
Internal pull-down 20K is disabled after FLRST

HDA SDO

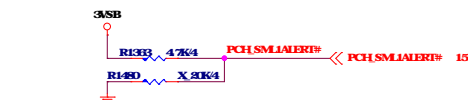
ME flash by Q10

PCH HIGH PCH side

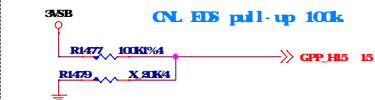
15 ME_DIS#



Reserved



Reserved



MICROSTAR INT'L CO., LTD

MS-7009

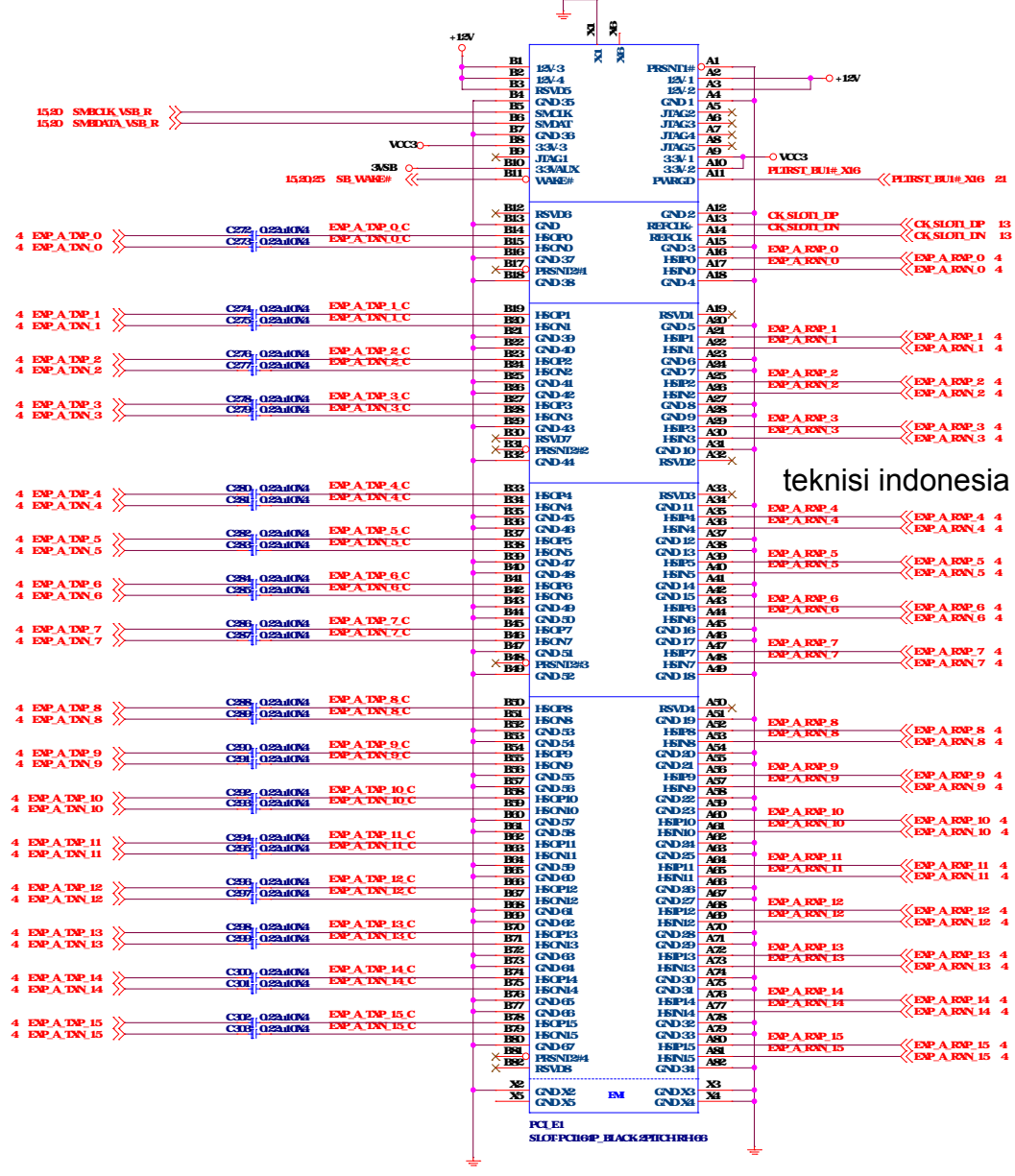
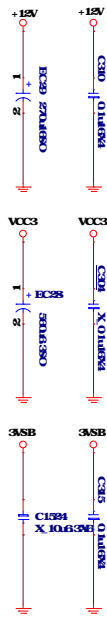
Site
Custom

Document Description
PCHSwap

Date: Tuesday, March 24, 2020

Sheet 18 of 22

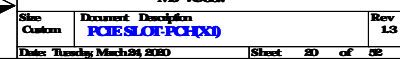
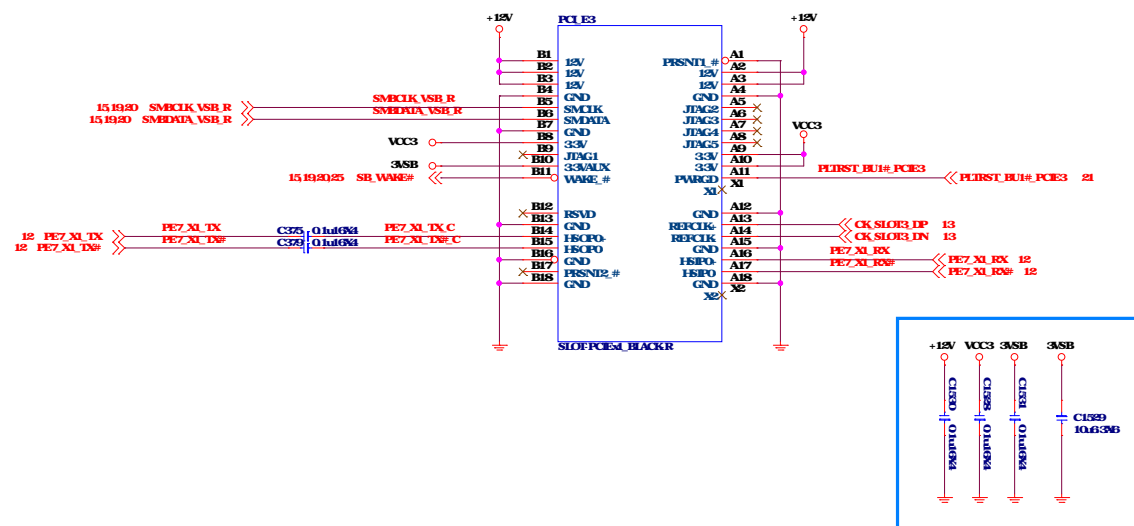
Rev
1.3



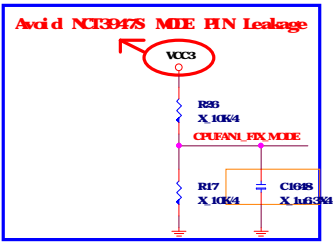
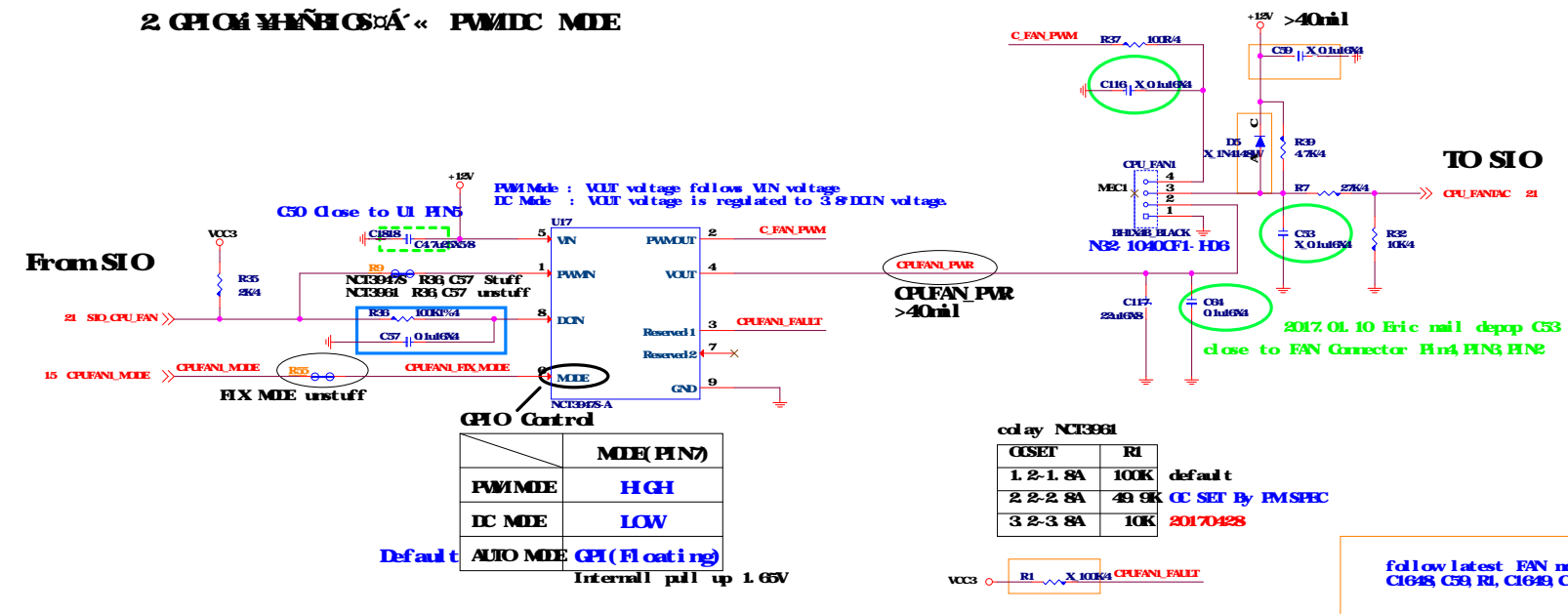
teknisi indonesia



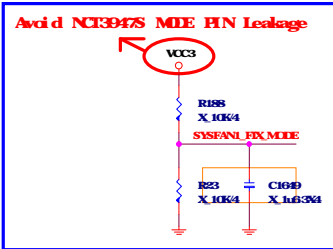
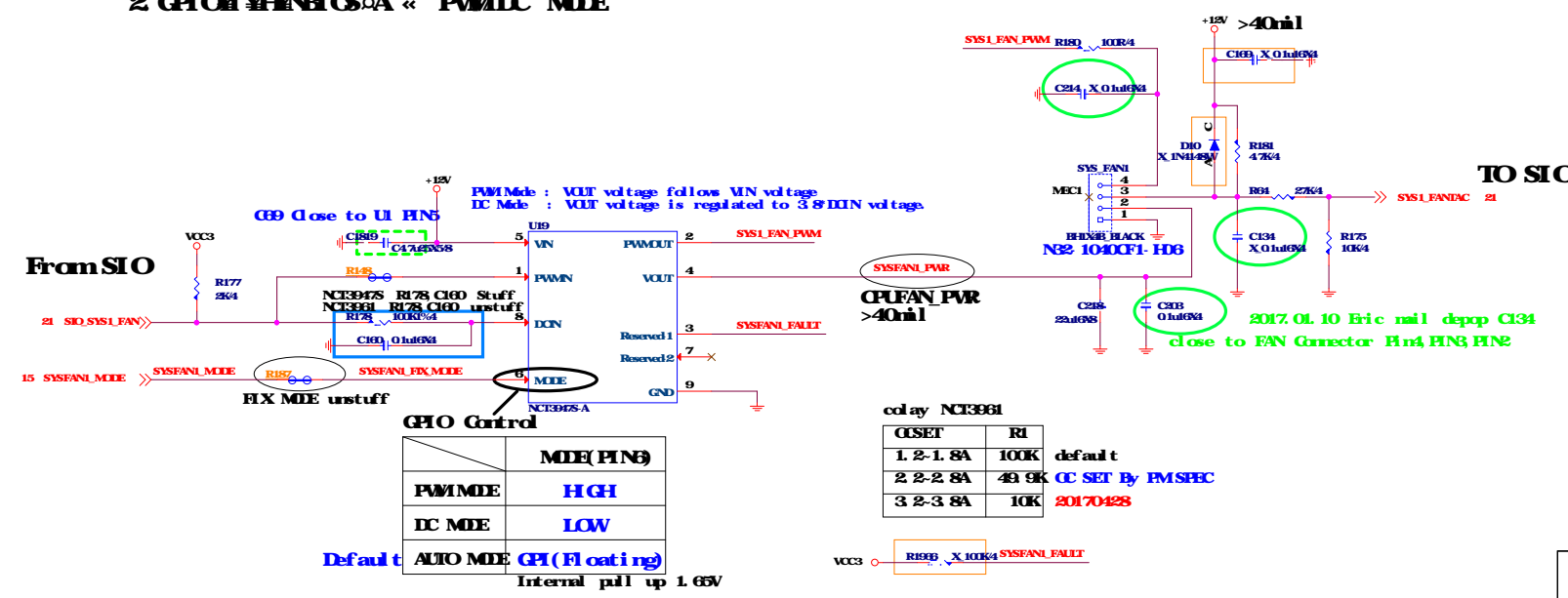
MICROSTAR INT'L CO., LTD			
MS-700B			
Site	Document	Revision	Rev
Custom	PCIE SLOT CPU X16	1.0	1.0
Date: Tuesday, March 24, 2020		Sheet	30 of 32

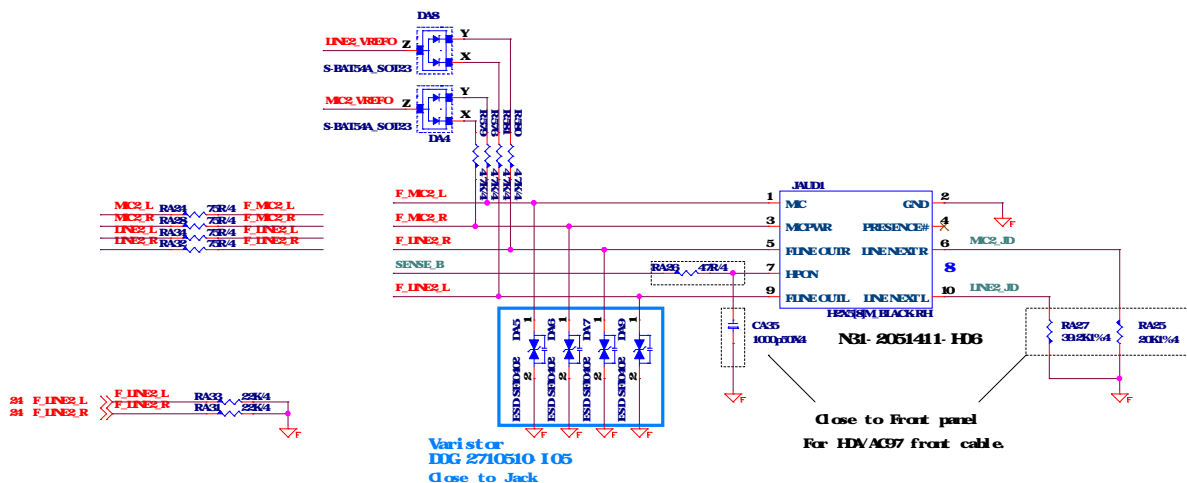
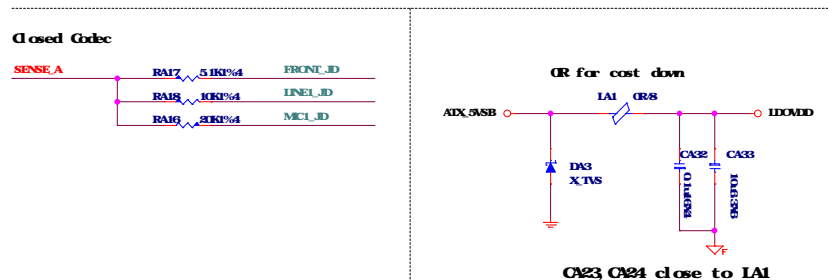
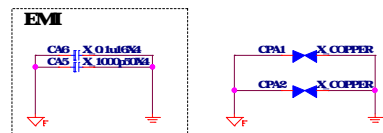
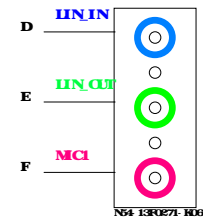
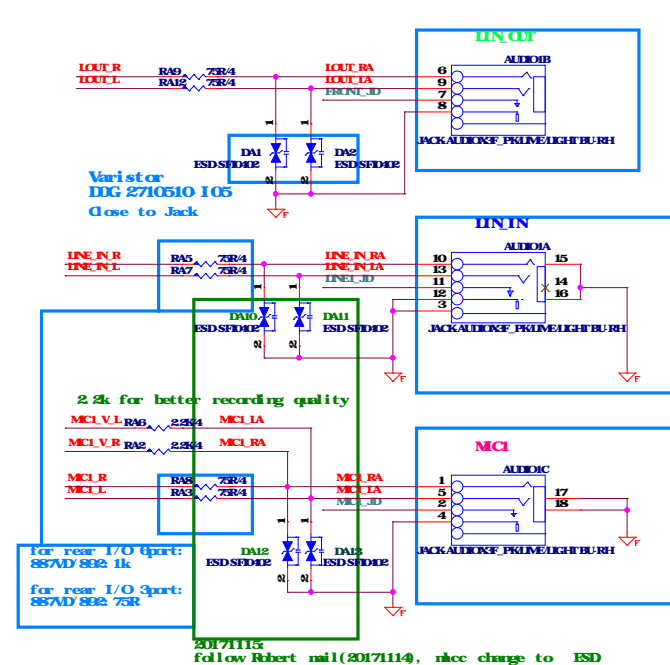
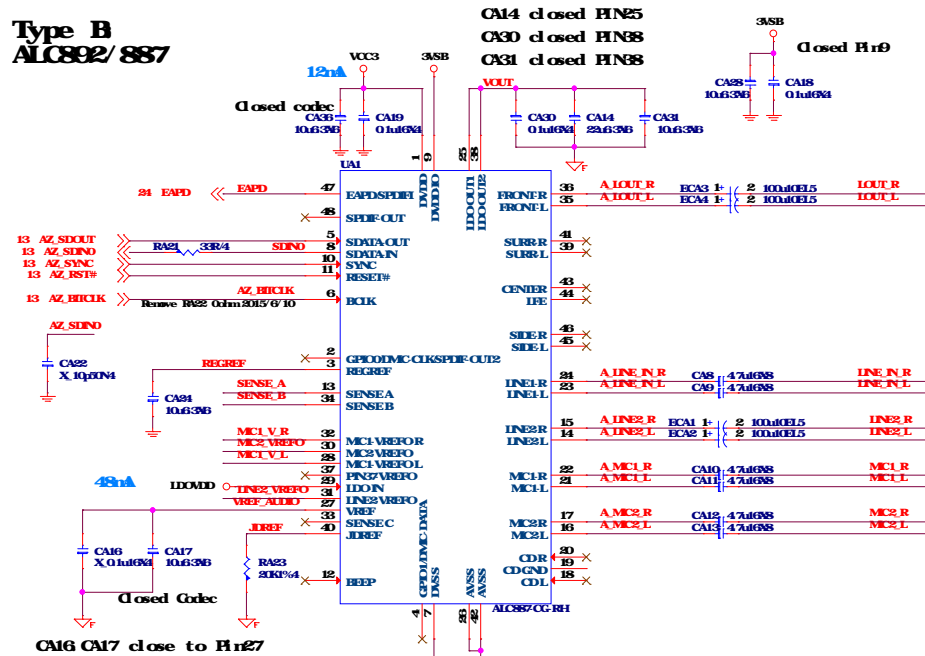


TYPE K: 4 PIN CPU FAN USE NCI3947S USE PCH GPIO CONTROL FAN MDE
 2 GPIO MDE HINCSA « PWMDC MDE



TYPE K: 4 PIN CPU FAN USE NCI3947S USE PCH GPIO CONTROL FAN MDE
 2 GPIO MDE HINCSA « PWMDC MDE



Type B
ALC892/ 887

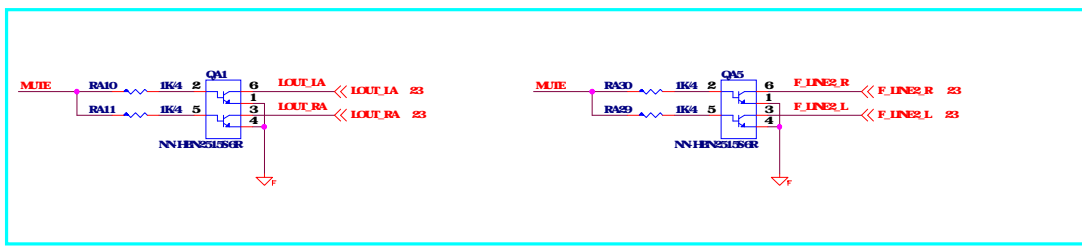
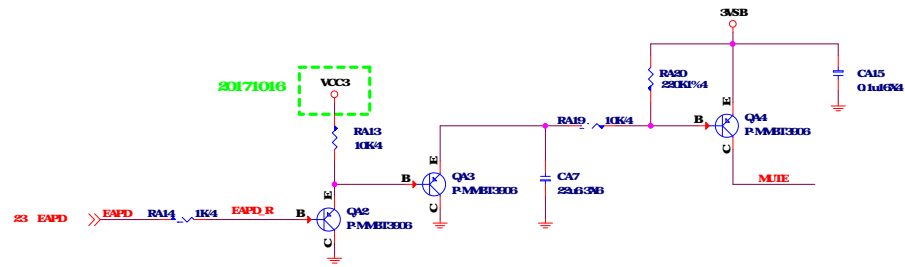
MICROSTAR INT'L CO., LTD

MS-7009.

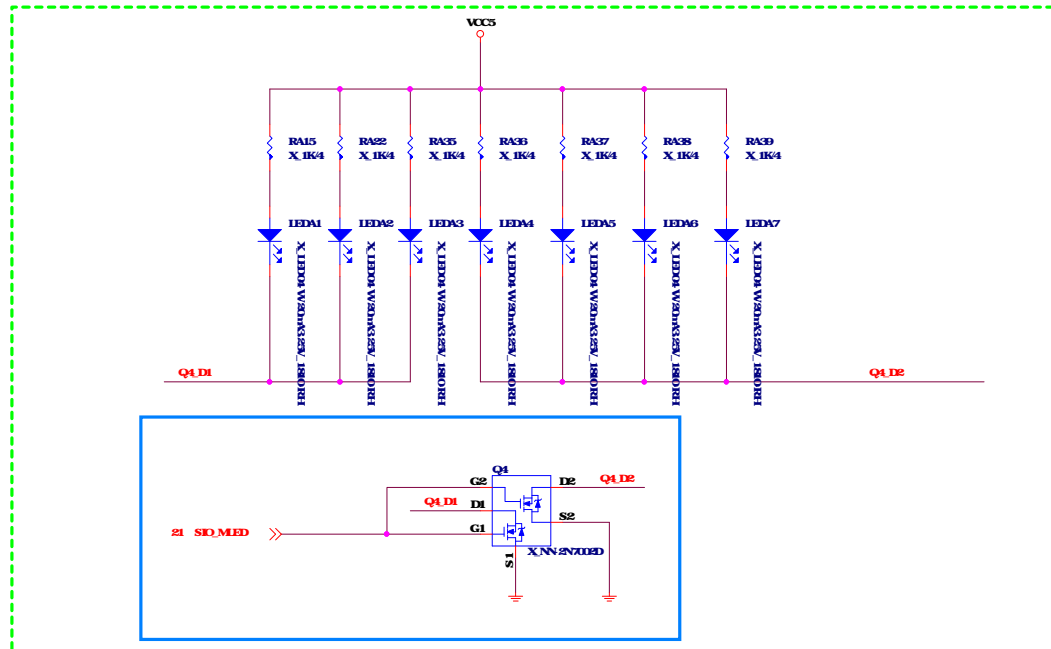
Size Custom	Document Description ALDIO-ALC89288
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Date: Tuesday, March 24, 2020		Sheet 23 of 52
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ear in e circuit



ufo



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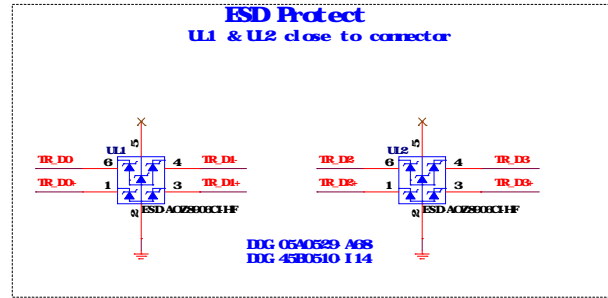
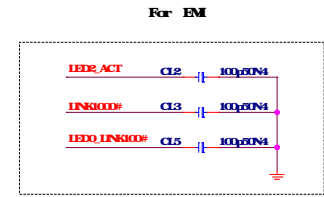
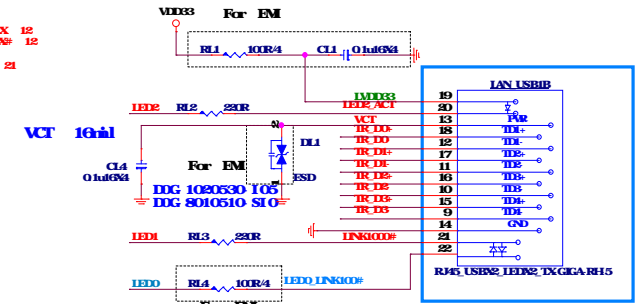
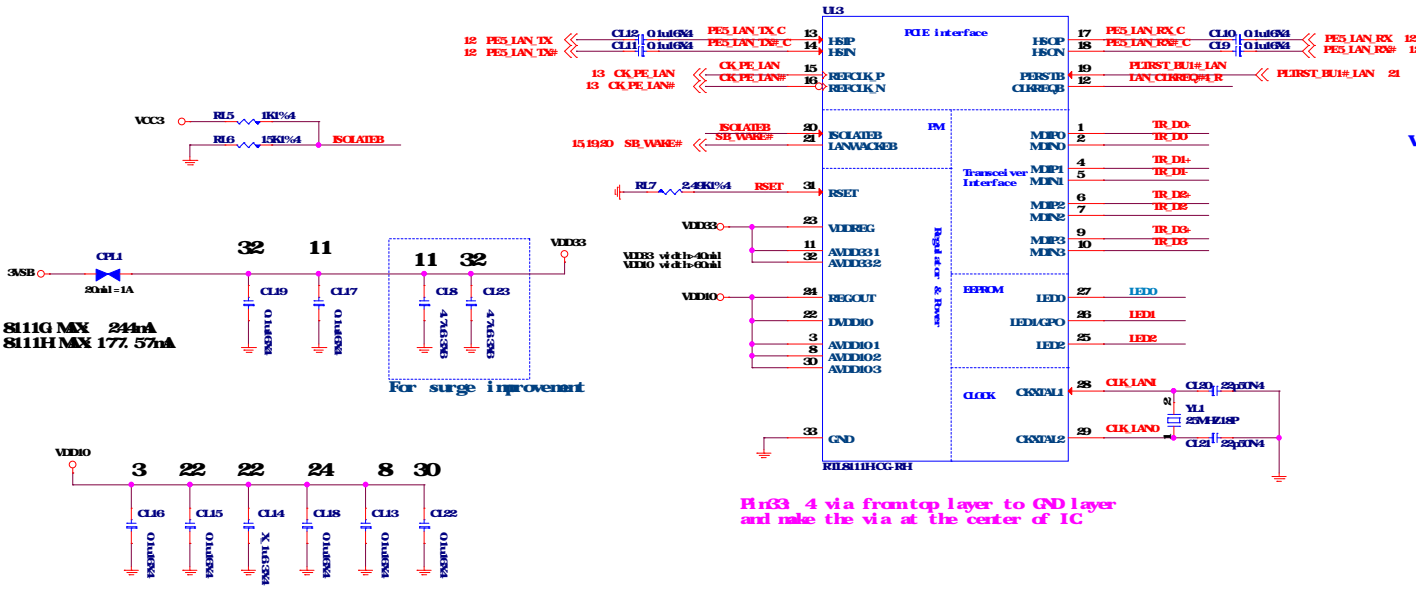
MICROSTAR INT'L CO., LTD		
MS-700B		
Site	Document	Revision
Custom	ALDO- dypcircuit	1.0
Date: Tuesday, March 24, 2020		Sheet 24 of 25

RIL811G/RIL811H Giga LAN

811H B08 0811CC R09
811G B08 08116C R09

LAN_CLKREQ#4,R R10#4 >>> LAN_CLKREQ#4 I3

LAN Connector



811G POWER Consumption

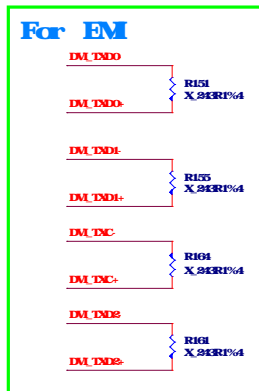
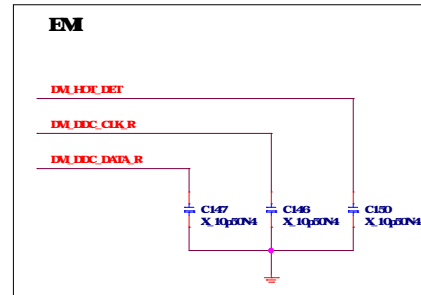
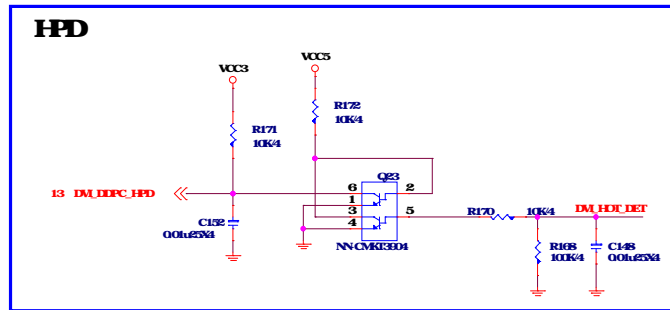
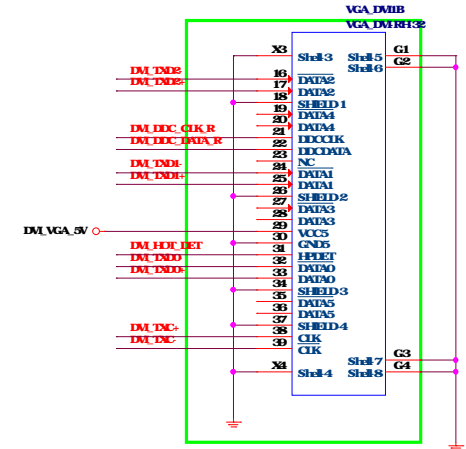
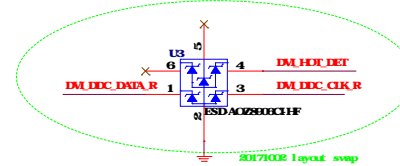
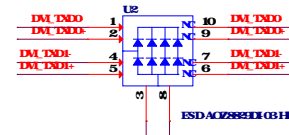
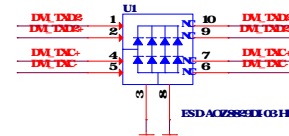
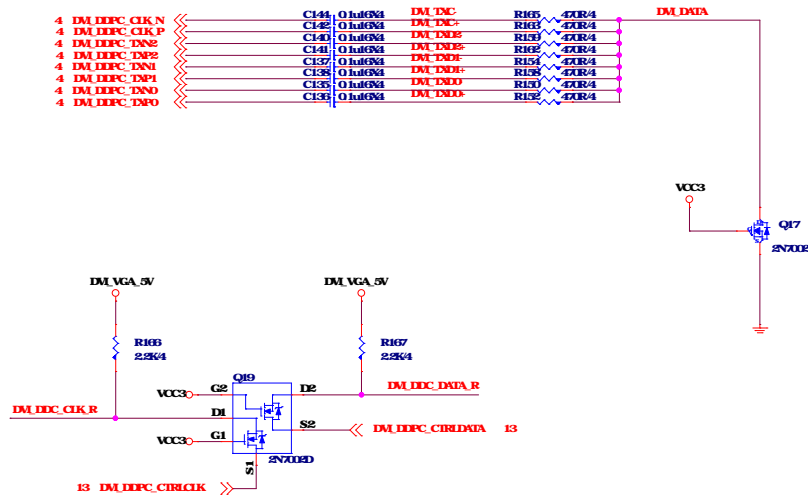
	3.3V @ mA	mW
10 Mbit/s/Tx&	17.15/116.7	56.6/385.1
100 Mbit/s/Tx&	71.45/129.5	235.8/427.4
Giga Tdc/Tx&	179.1/243.9	591/804.9
ALPS	6.41	21.15

811H POWER Consumption

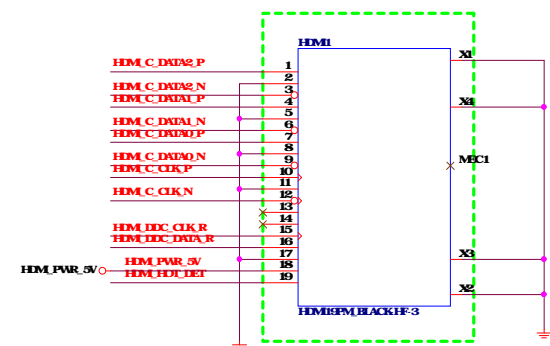
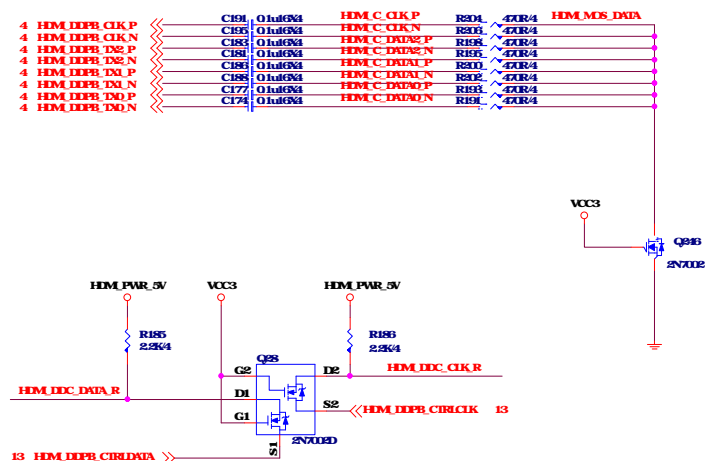
	3.3V @ mA	mW
10 Mbit/s/Tx&	9.9/84.69	32.67/279.48
100 Mbit/s/Tx&	48.11/92.44	158.76/305.05
Giga Tdc/Tx&	124.5/177.57	410.85/585.98
ALPS	5.50	18.15

DM level shifter

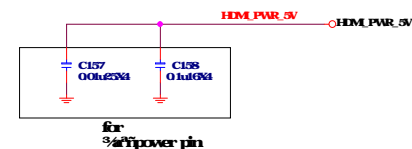
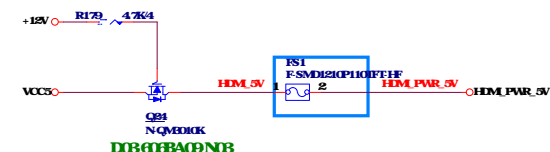
VGA resolution of 2048x1536 pixels with 32 bit color at 75 Hz (4:3 QGA)



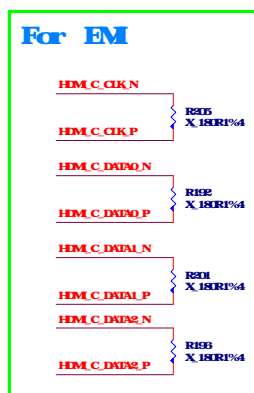
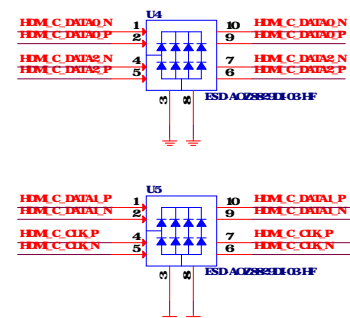
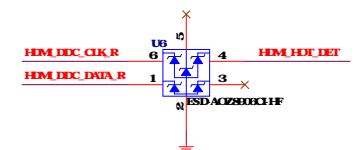
HMI, DM : 1920x1200 at 60 Hz (16 10 VNGA)



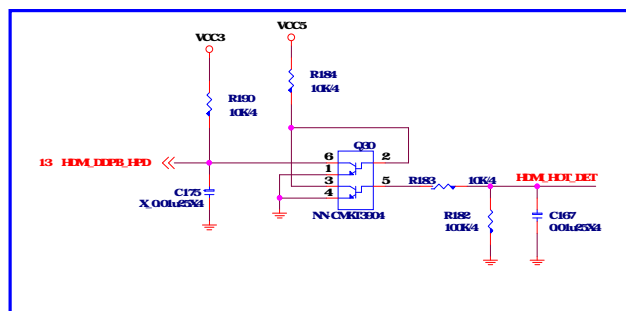
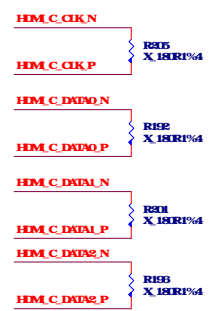
Vinafix.com



for 5V power pin



For EM



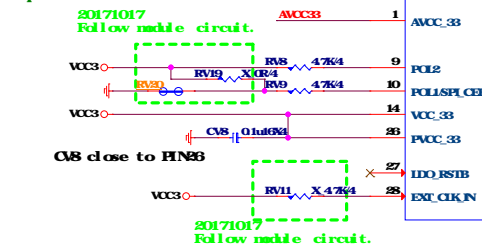
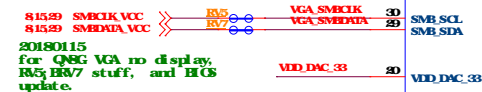
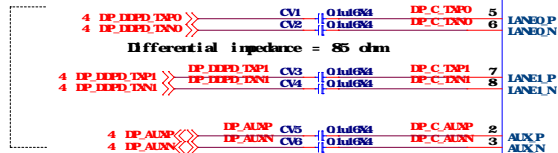
Note:

If connect to eDP port, must confirm whether it support hot plug detection and re-audstraining

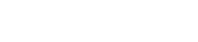
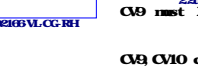
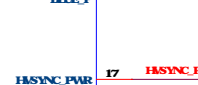
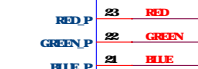
20171130

UI05 -> HUB 02166C R09 change R G B internal driving

UI05



RID2166



20171017 Follow module circuit. DM_VGA_5V -> VCC5

20171019 CV27, unify 20K > 10K

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

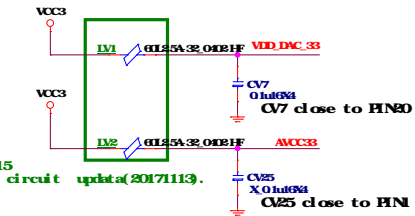
Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

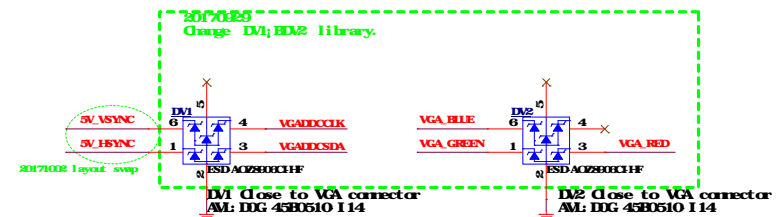
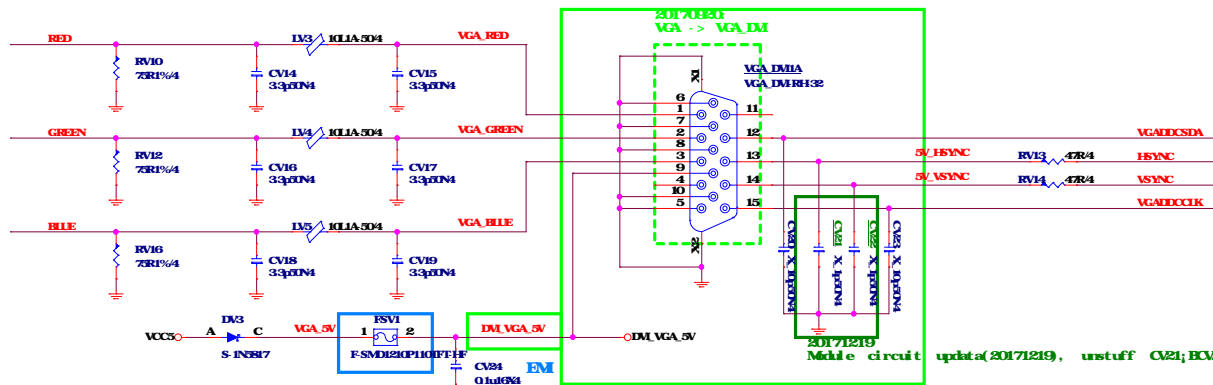
Q27, Q27 close to HIN7

Q27, Q27 close to HIN7

VCC3 Full Screen current 165mA



RID2166 SMBus address is 68h



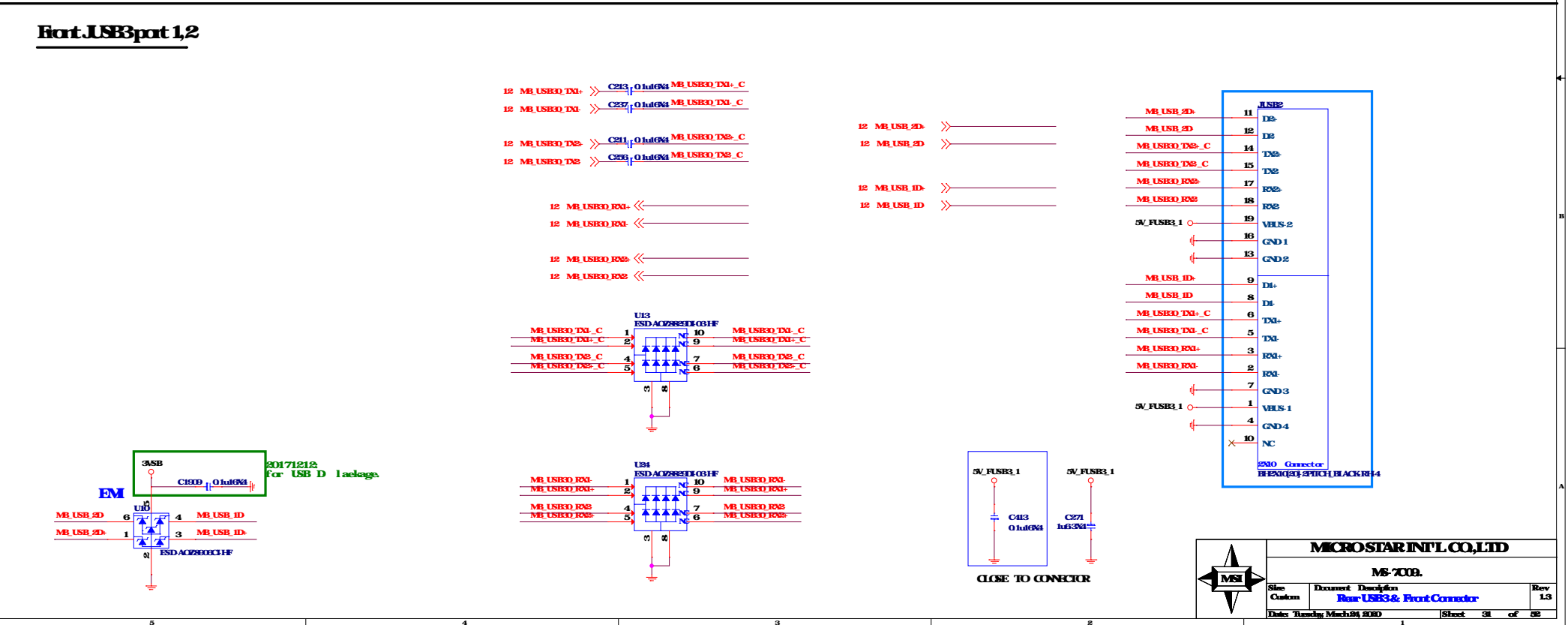
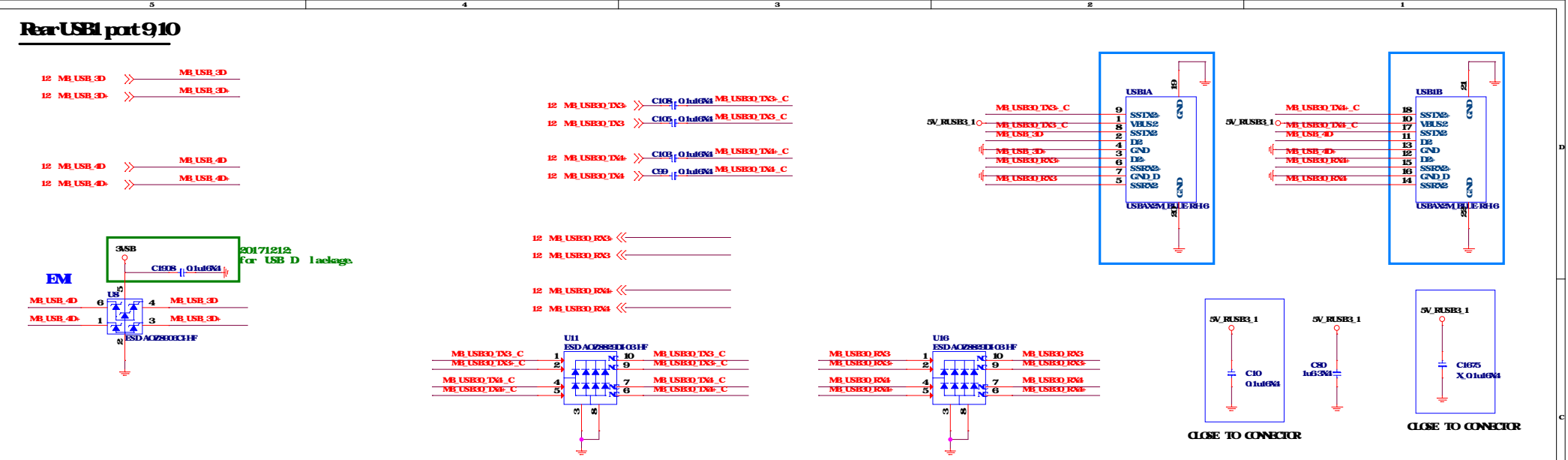
Mit ID8 0100800 P16
Av1: ID8 0100200 B07

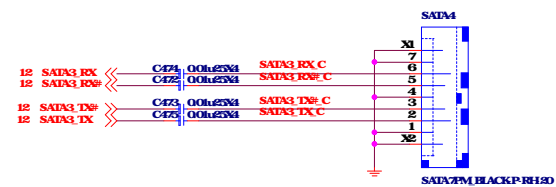
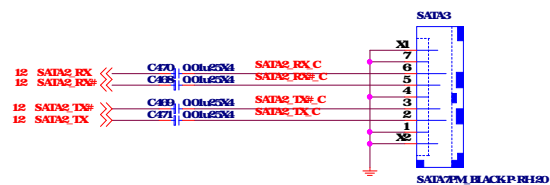
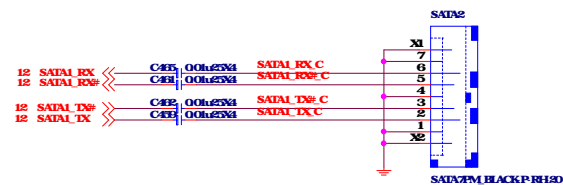
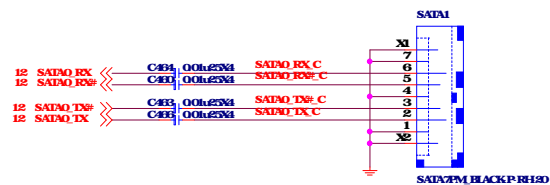


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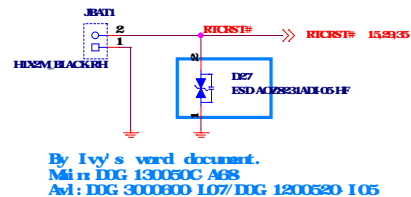
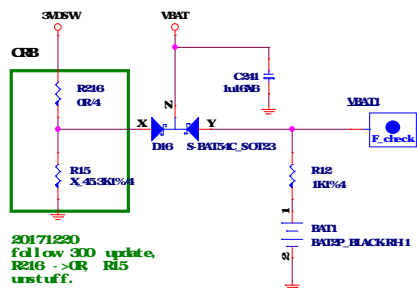
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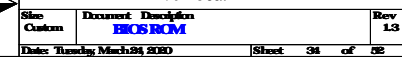




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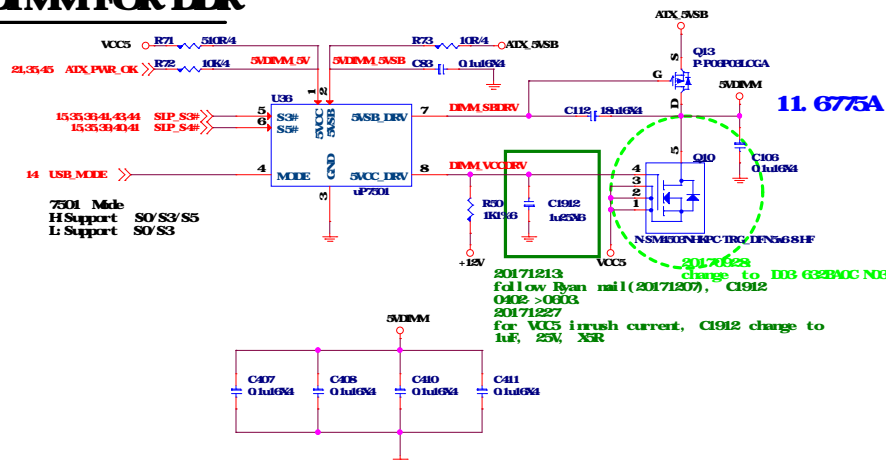
VBAT



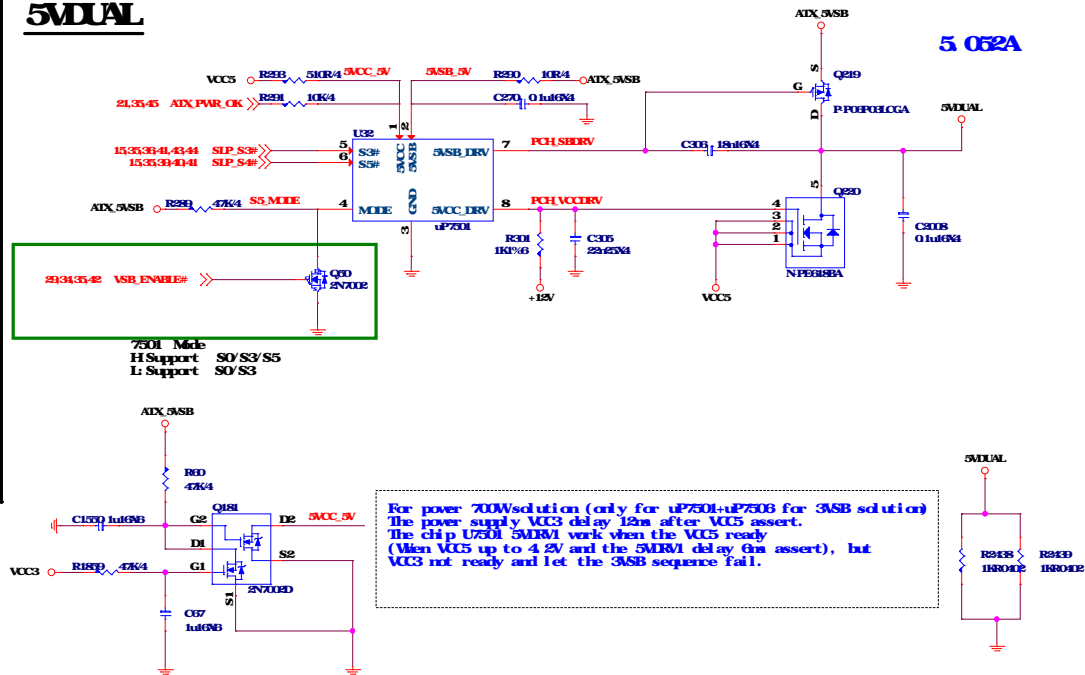


5VIMM FOR DDR

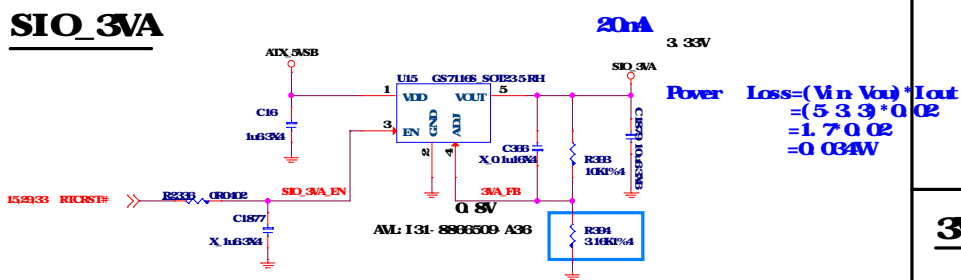
(3A for DDR 6 GA for USB)



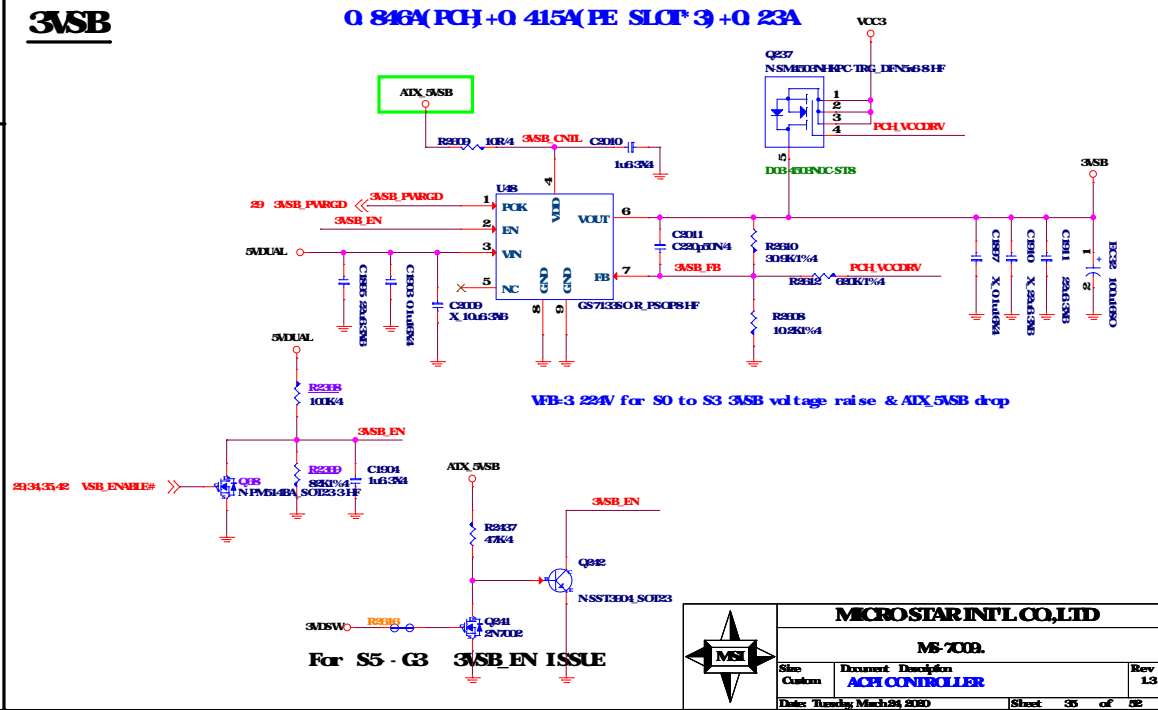
5VDUAL



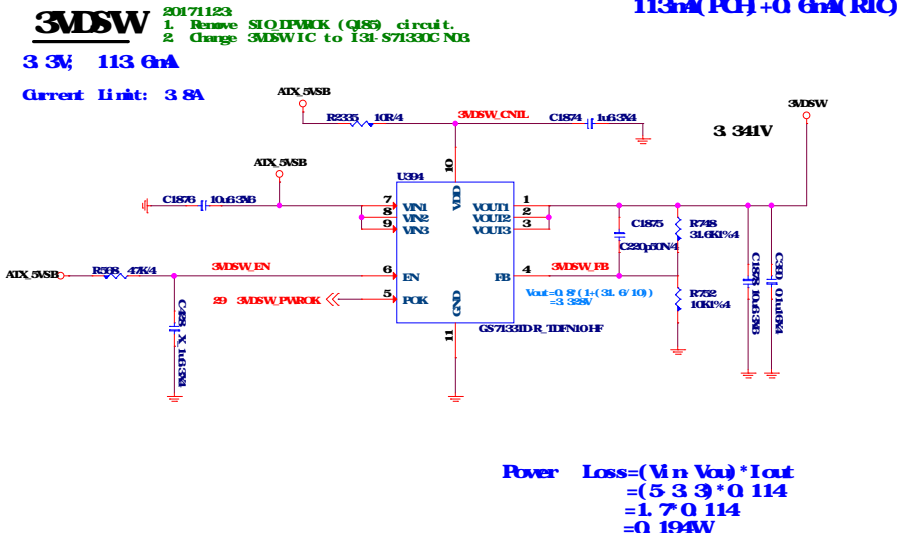
SIO_3VA



3VSB



3VSW

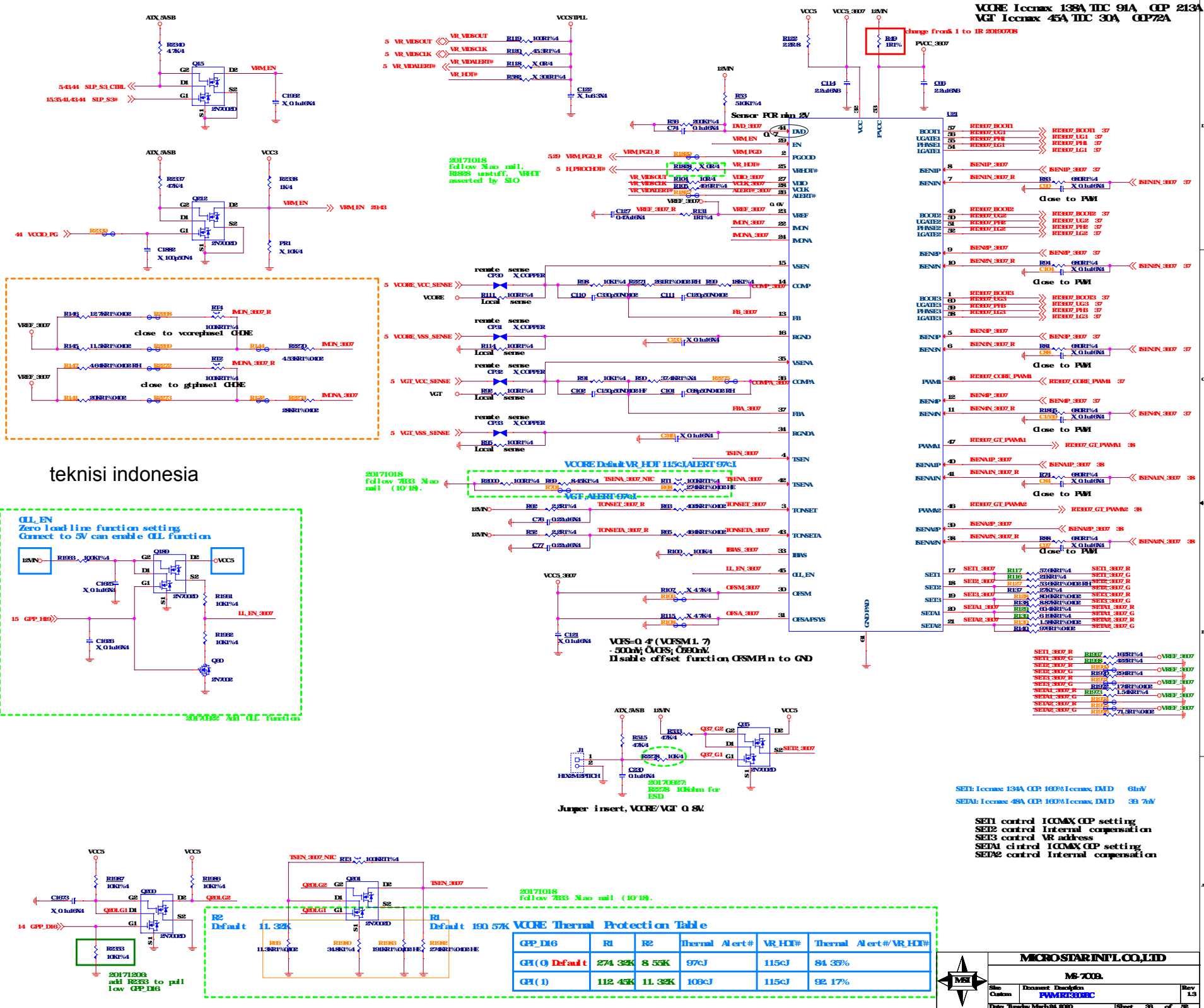


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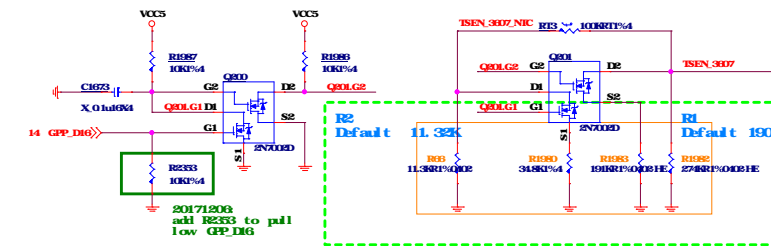
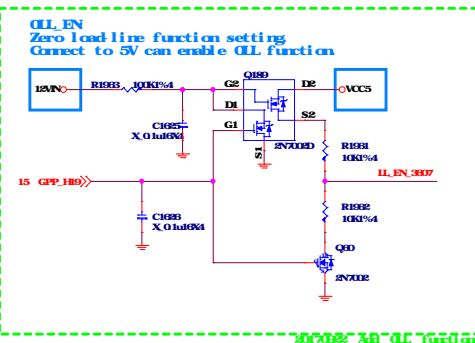
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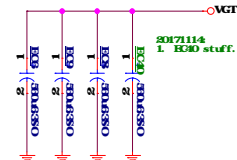
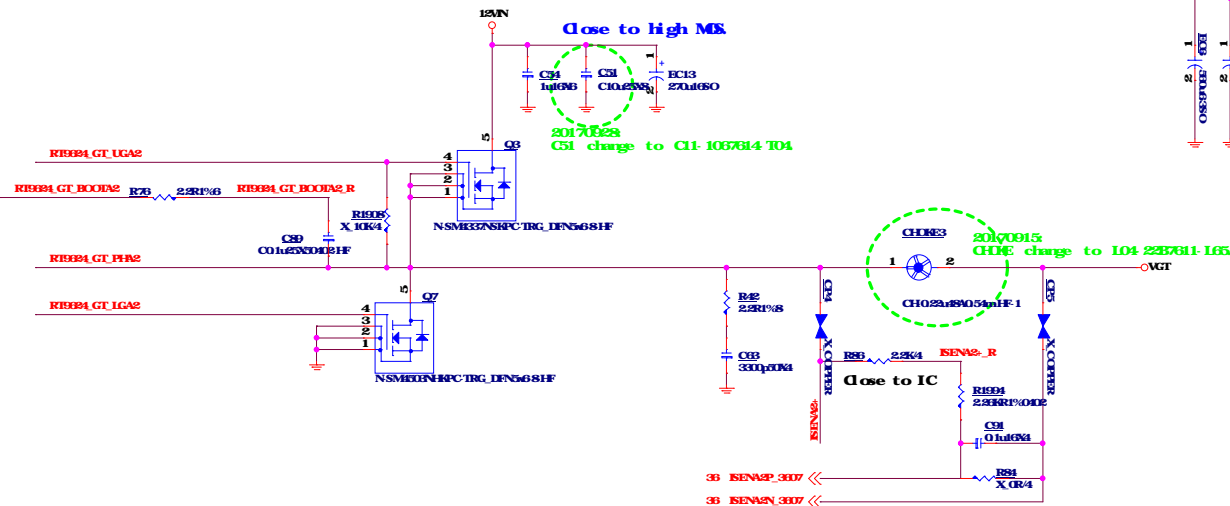
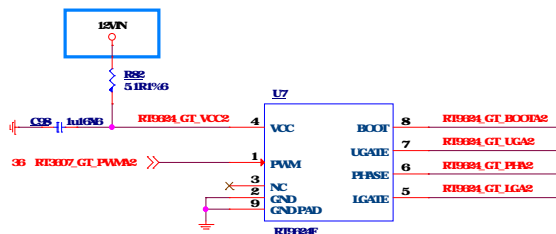
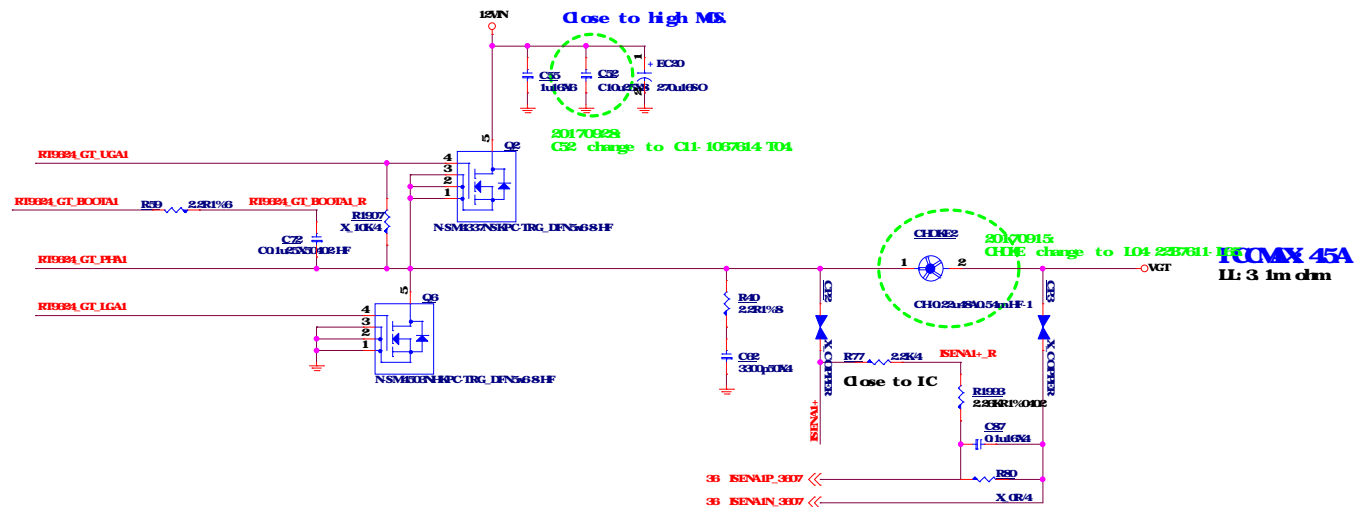
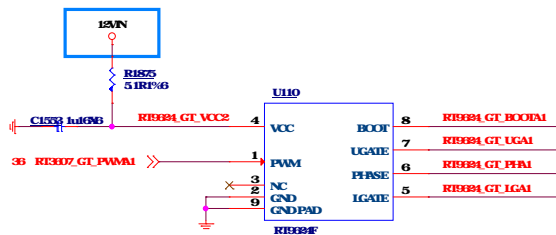


20171018 follow 7833 Xiao mail (10/19).

WORE Thermal Protection Table

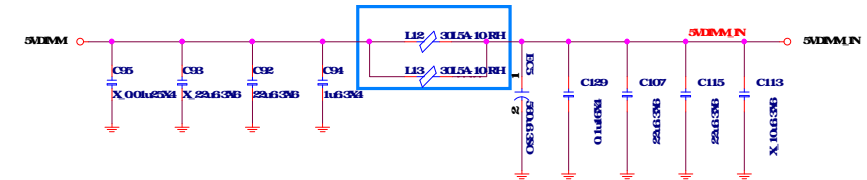
GPP DiG	R1	R2	Thermal Alert #	VR HOT#	Thermal Alert #/VR HOT#
GPI (0 Default)	274 32K	8 55K	97°C	115°C	84 39%
GPI (1)	112 45K	11 32K	108°C	115°C	92 17%





VCC_DDR

VD	Reference Voltage (V)
H	0.675
L	0.75

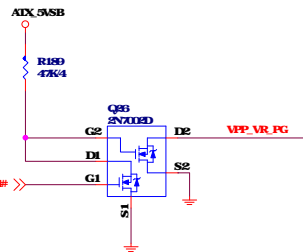
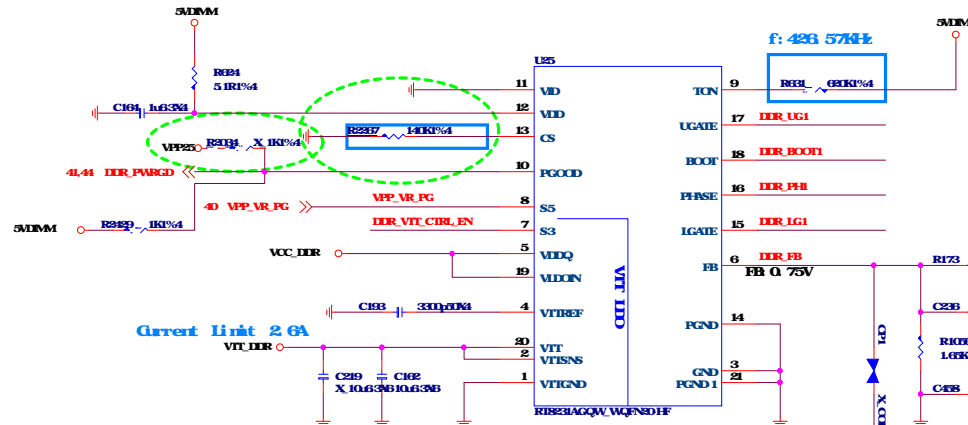


$$I_{rrm} = I_{out} \cdot \sqrt{V_{out}/V_{in}} \cdot (1 - (V_{out}/V_{in}))$$

$$= 9.525 \cdot 0.427$$

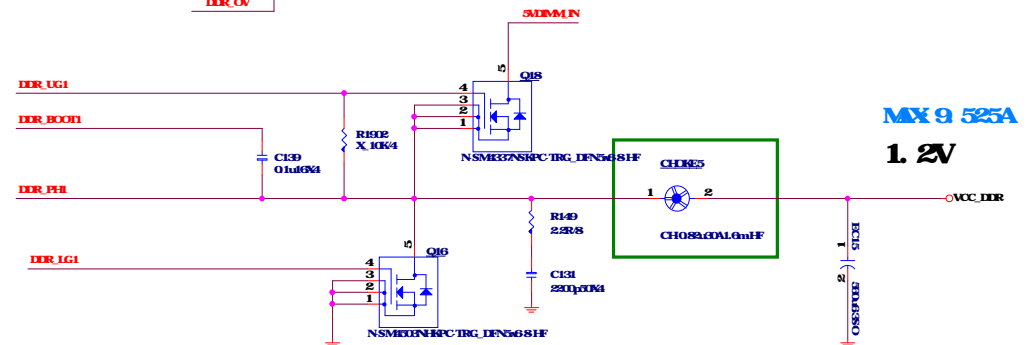
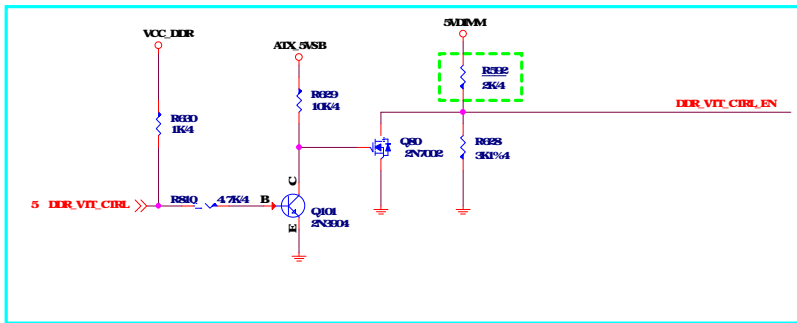
$$= 4.06797A$$

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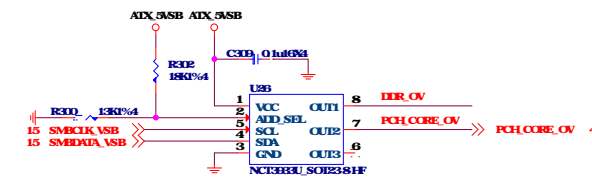
SIP.S4# de assertion to VDDQ ramp down start

VP ramp down after VDDQ ramp down



UPI VOLTAGE CONSOL

0.2G R4=18K RL=13K



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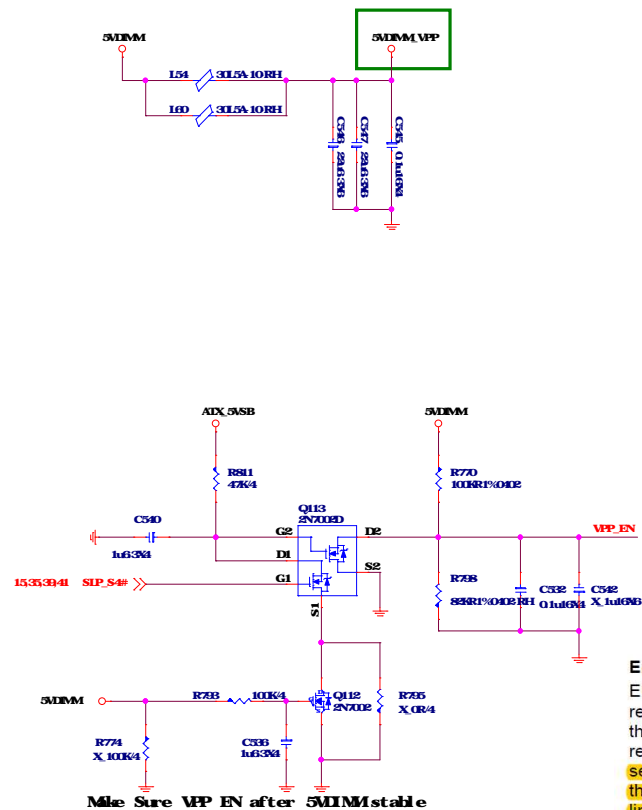
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2DIMM: 1.12A FOR DDR VPP2 5V

VPP25 Power 2.5V, 2A



ENABLE HIGH 1.16-1.29V

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 40µA to prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V V_{IN} , $I_{Zener} = (12V - 2.8V) / (604k\Omega + 35k\Omega) = 14\mu A$.

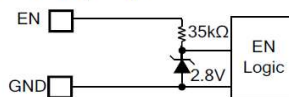
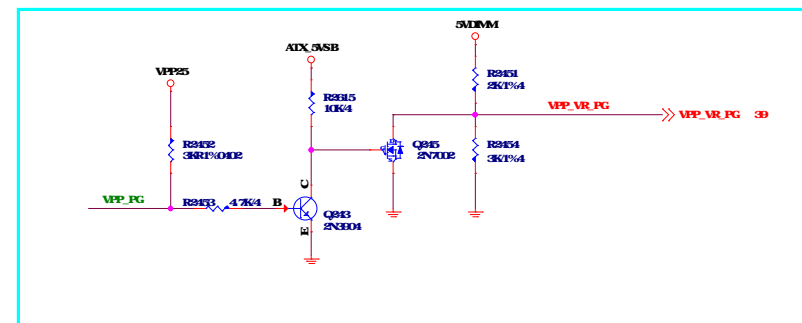
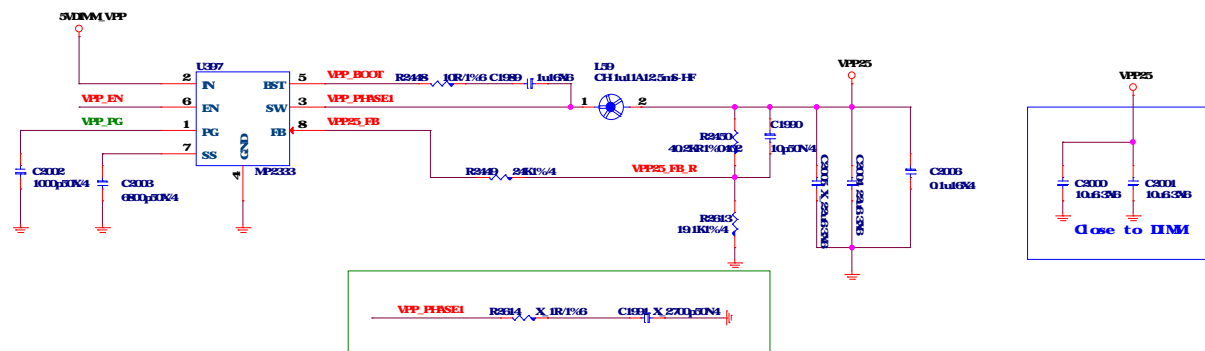


Figure 2: Zener Diode between EN and GND



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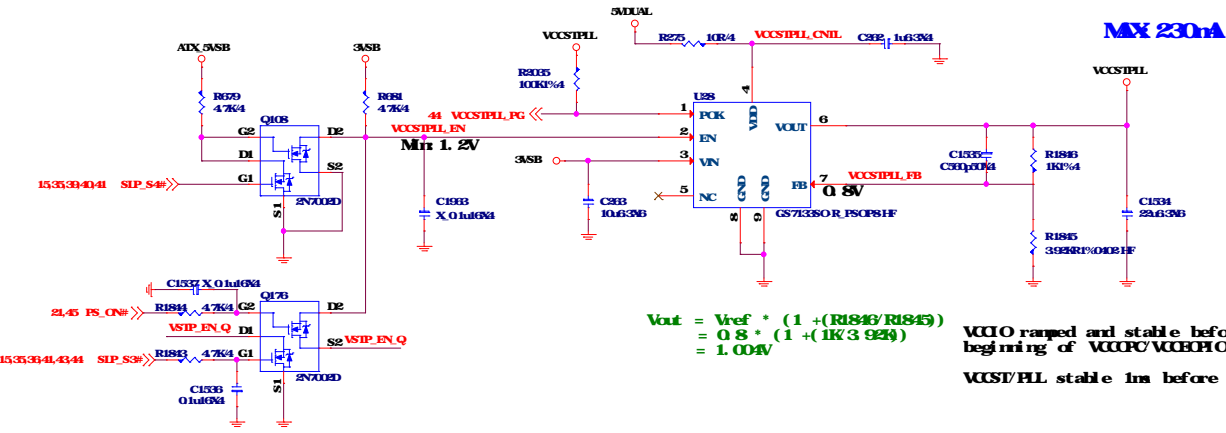
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VCCSTPLL

1.0V; 230mA



Power Loss=(Vin-Vout)*Iout
=(3.3-1.0)*0.23
=2.3*0.23
=0.529W

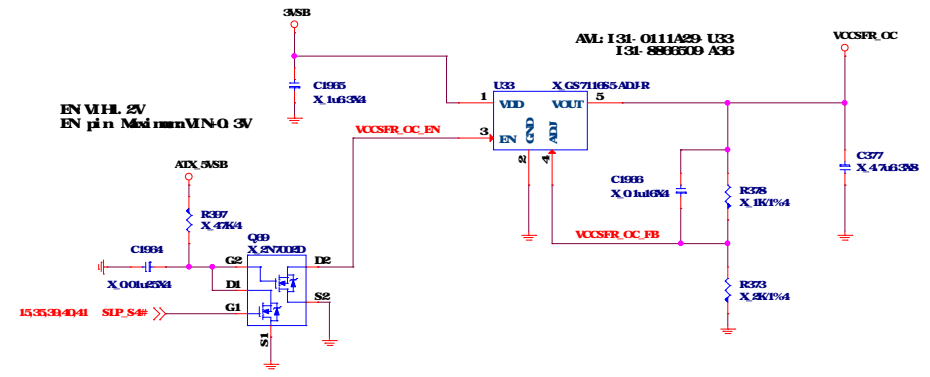
Vout = Vref * (1 + (R1846/R1845))
= 0.8 * (1 + (1K/3.92K))
= 1.004V

VCCIO ramped and stable before
beginning of VCCIO/VCCSTIO ramp
VCCST/HL stable 1ms before PROPMG

VCCPLL_OC

1.2V; 130mA

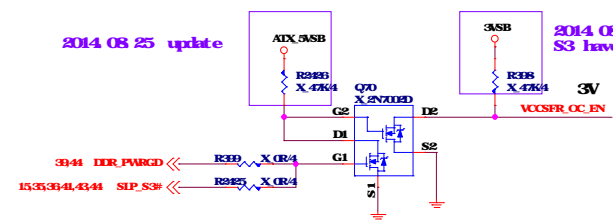
Power Loss=(Vin-Vout)*Iout
=(3.3-1.2)*0.13
=2.1*0.13
=0.273W



2014 08 21 update

2014 08 25 update

2014 08 25 update
S3 have power



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1.05V, 10.285A

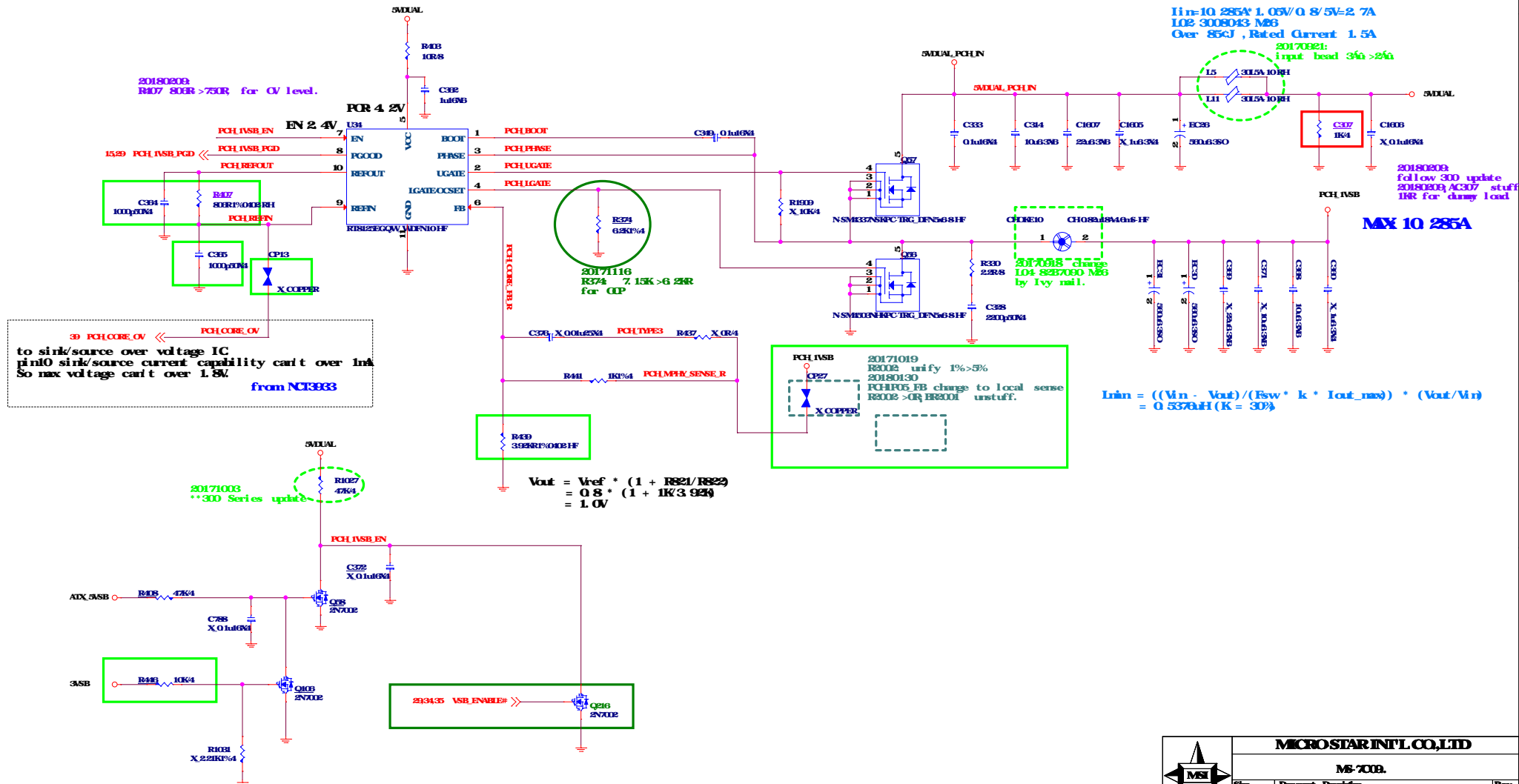
Rocpset: 5 6K
OCF(nin)=Rocset*Iocset/Rdson(Low side)
=6 2K 10uA/ 5. 1mahm
=12 16A

$$\begin{aligned} OCP_{(max)} &= R_{ocset} * I_{ocset} / R_{ds(on)} (Low \text{ side}) \\ &= 6.2k * 10uA / 3.9m\Omega \\ &= 15.90A \end{aligned}$$

Rison (low) 5V
DOB 450NOC ST8
Max 5 1nahm Min 3 9nahm

$$\begin{aligned} I_{rms} &= I_{out} * \text{SQRT}((V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))) \\ &= 16.685 \text{ } 0.407 \\ &= 6.79 \text{ A} \end{aligned}$$

I_m=10 285A* 1.05V/0.8/5V=2.7A
 L02 3008043 M26
 Over 85°CJ , Rated Current 1.5A
 20170921:
 input bead 340 >240



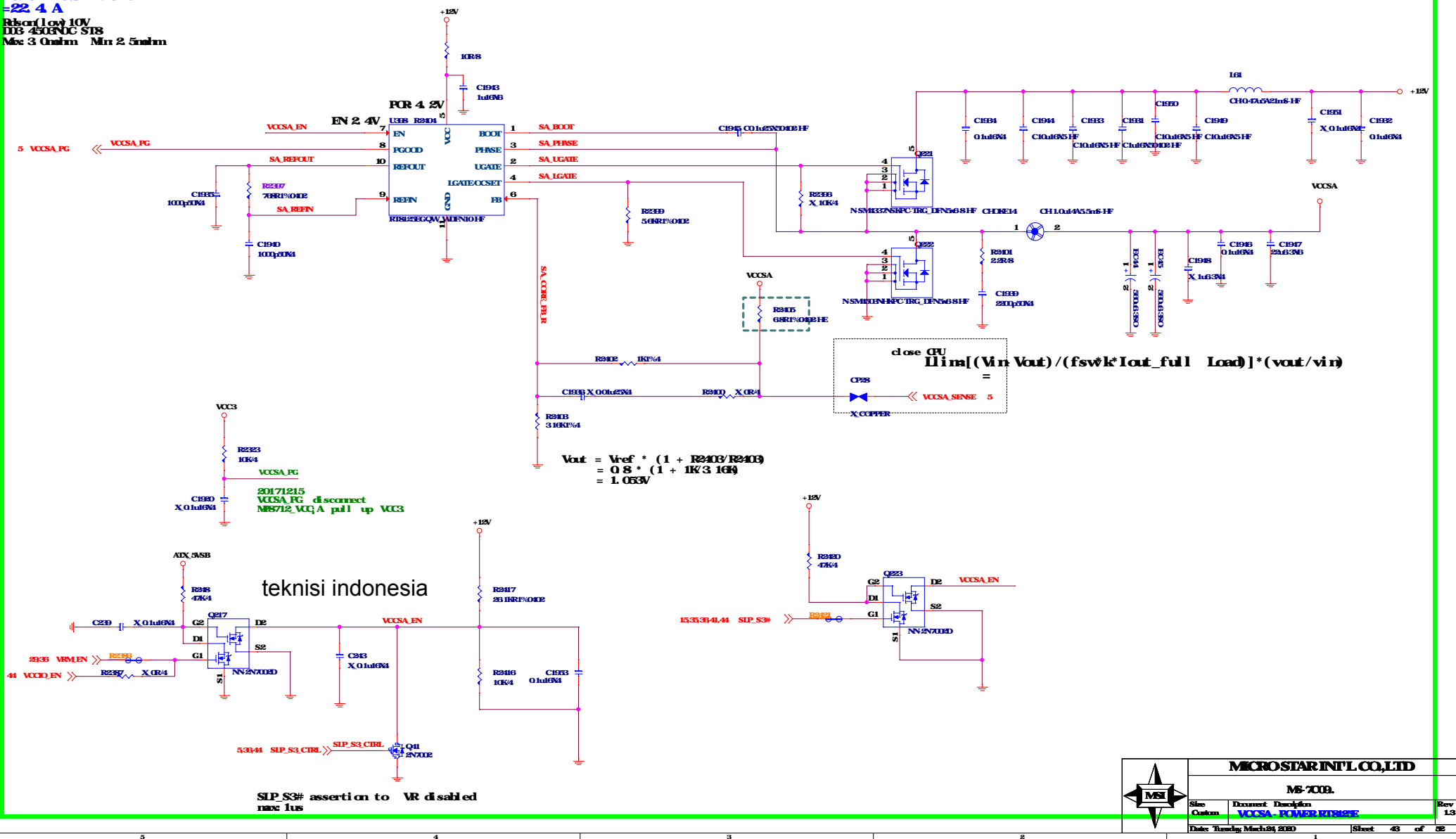
SA Power: 1.05V, 11.1A

$$I_{rms} = I_{out}/N * \sqrt{R_{DS(on)} / (1 - D)}$$
$$= 12.3 * \sqrt{0.0875 / 0.9125}$$
$$= 3.47A < 5000mA$$

$$R_{ocpset} = 5.6K$$
$$OCP(min) = R_{ocpset} * I_{ocset} / R_{lson}(Low\ side)$$
$$= 5.6K * 10uA / 3.0uA$$
$$= 18.67A$$


$$OCP(max) = R_{ocpset} * I_{ocset} / R_{lson}(Low\ side)$$
$$= 5.6K * 10uA / 2.5uA$$
$$= 22.4A$$

$R_{lson}(Low)$ 10V
D03 450mDC S18
Max 3.0uA Min 2.5uA

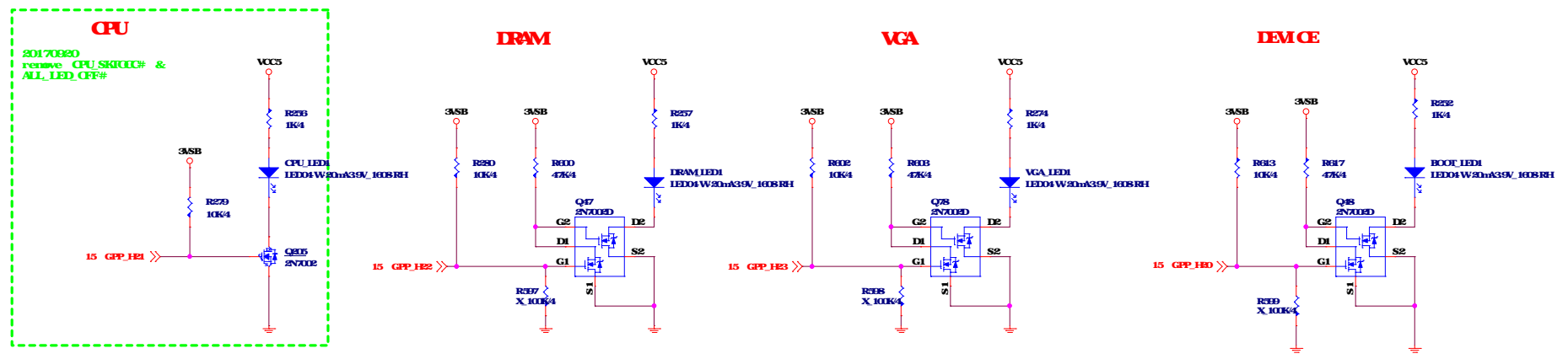


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SLP S3# assertion to VR disabled
max 1us

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DEBUG LED




LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
«G	NAIIVE	GPO	GPO	NAIIVE
•À	NAIIVE LOW	GPO LOW	GPO LOW	GPO LOW

LED
RED DDC 040P100 H91
AM: DDC 040S500 E07

WI: DDC 040I200 H91
AM: DDC 040S200 E07

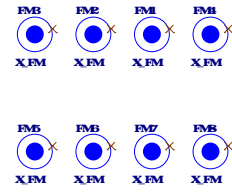
1. CPU check CPU LED «G» A check PASS «A» h CPU LED A ± 1/4 C
2. Memory / memory LED check PASS «A» h memory LED A ± 1/4 C
3. VGA check VGA LED «G» A check PASS «A» h VGA LED A ± 1/4 C
4. AT LED check AT LED «G» A check PASS «A» h AT LED A ± 1/4 C

EM CAP

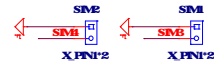


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Optical Fiducial Marks-120



Simulation



Mounting Holes

